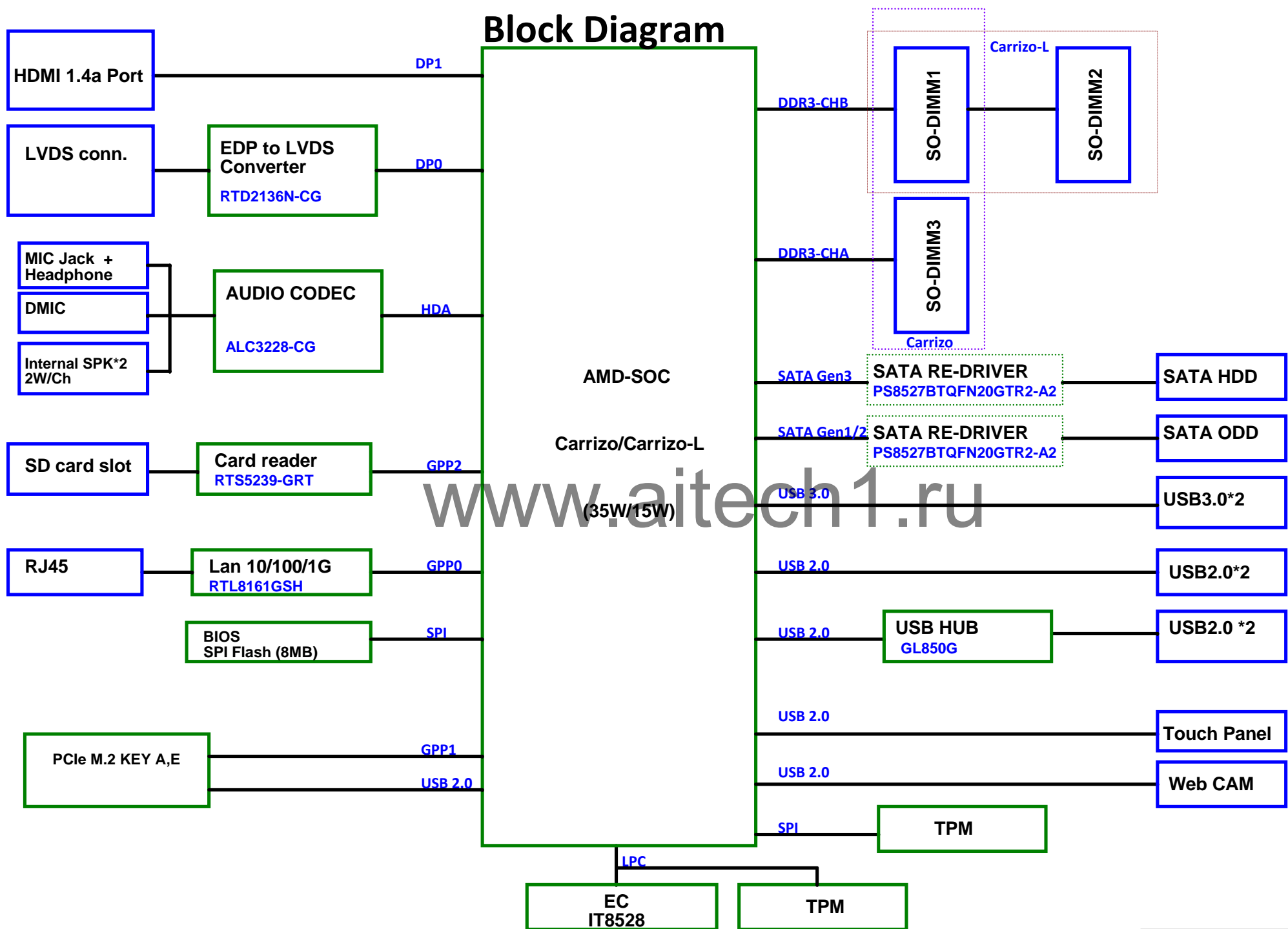


Block Diagram



54321

SI to PV Change List

EC-PV-E01 SWAP USB touch and camera for touch no function issue

EC-PV-E02 Add APU_VDDNB_RUN_PB_L

EC-PV-E03 Change D15 to AZ4212 to meet 12V

EC-PV-E04 Delete USB signal 0ohm of reserve

EC-PV-E05 Change U39 to G517G1P81U(MSOP8) for max current to 3A.

EC-PV-E06 Depop C255 and change footprint to 0402 for sequence fine tune and unified 1uF size.

EC-PV-E07 Change L11 footprint for SMT request.

EC-PV-E08 Reserve change backlight sequence for panel flash when panel power off

EC-PV-E09 Change 0ohm to short pad location R39,R58,R59,R45,R348,R91,R92,R364 ,R69,R70,R71,R72,R73,R74,R120,R169,R173,R432,R541,R542,R382,R383,R389,R392,R406,R415, L16,R164,R166,R414,R421,R426,R210,R226,R228,R229,R230,R232,R233,AR3,AR35,R471,R208, R457,R216,R275,R296,R297,R298,FR1,FR2,FR3,FR4,FR5,FR6,FR7,FR8,R250,R84,R85,R89,R305 ,R313,R314,R315,R316,R318,R96,R106,R260,R261,R199,R184,R186,R543,R458,R320,AR4,AR7, F1,L27,AR30,AR6,R254,P6,F5,P3

EC-PV-E10 Change AD3,AD4,AD6,AD7 footprint for SMT request

EC-PV-E11 Add GND pad H17 for EMI request.

EC-PV-E12 Add short pad G2 on EC pin31 for reset panel ID.

EC-PV-E13 Pop AR19,AR27,AR28,AR36 to 0.47uF for ESD solution.

EC-PV-E14 Change D14,D17,D18,D20,D21,D34 footprint for SMT request.

EC-PV-E15 Change LED2,LED3 footprint for SMT request.

EC-PV-E16 Change Board ID to PVT1

EC-PV-E17 Change D7,D8,D9 from BC512501Z00 to BC052301Z00, Pop D36,D37 P/N BC052301Z00 for ESD request.

EC-PV-E18 Change R258 form 0603 to 0402 Unifile with DC-IN LED

EC-PV-E19 Add EC_PCA_ID for PCA_ID identify

EC-PV-E20 Depop TPM relate material PV stage depop reserve material

EC-PV-E21 Change R178 from 680ohm to 619ohm for USB eye diagram

EC-PV-P01 Change 0ohm to short pad location PR157,PR150,PR274,PR103,PR226,PR228,PR243 ,PR96,PR97,PR98,PR211,PR212,PR182,PR52,PR53,PR4,PR9,PR11,PR10,PR30,PR26,PR81,PR82,PR54,PR56,PR70,PR62,PR63,PR37 ,PR38,PR138,PR17,PR35,PR20,PR113,PR252,PR125,PR116,PR199

EC-PV-P02 Change PC239 footprint to 0603 change footprint for buyer suggest

EC-PV-P03 Add 0402 cap reserve 0402 cap

EC-PV-P04 Change MOS PQ38 for high side Mos temperature Rds-on from 26m ohm to 11.7m ohm in 4.5V

EC-PV-P05 Remove reserve material PD2,PC115,PR172,PR171,PR176,PR174,PC116,PR170 remove AC_Lost cirucit

EC-PV-P06 Change CZ-L PR259 and PR261 value be same with CZ for 90W adapter ID and CPU throttling point.

www.aitech1.ru

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	+19V		Always
VCCRTC	+1.5V		Always
3V	+3.3V	S0_ON1_D	S0
3V_S3	+3.3V	SUSD	S0-S3
3V_S5	+3.3V	S5_ON_D	S0-S5
3V_AUX	+3.3V	AC/DC Insert enable	Always
5V	+5V	S0_ON1_D	S0
5V_S3	+5V	SUSD	S0-S3
5V_S5	+5V	S5_ON_D	S0-S5
5V_AUX	+5V	AC/DC Insert enable	Always
3V_WLAN	+3.3V	SLP_MINI	S0-S5
3V_LAN	+3.3V	LAN_PWR_ON	S0-S5
1.5V_S3	+1.5V	S3_ON	S0-S3
1.5V	+1.5V	S0_ON1_D	S0
1.8V_S5	+1.8V	S5_ON	S0-S5
1.8V	+1.8V	S0_ON1_D	S0
VDDP_S5	+1.05V	S5_ON	S0-S5
VDDP	+1.05V	S0_ON1_D	S0
VDDCR_FCH_S5	+0.775V	S5_ON	S0-S5
CPU_CORE	~	VRON	S0
NB_CORE	~	VRON	S0
12V	+12V	S0_ON1	S0
SMDDR_VTERM	+1.5V	S3_ON	S3

Schematic "Value" Definition

AMD Platform Compressor-U and Compressor-LU			DB/SI/PV Stage			MP		
By Value format	Description	Auto BOM Control	15W Carrizo-L	25W Carrizo-L	Carrizo	15W Carrizo-L	25W Carrizo-L	Carrizo
XX	Install	V	V	V	V	V	V	V
*XX	Non-Install	V						
CZ@XX	Install AMD Carrizo only	V			V			V
CZ-L@XX	Install AMD Carrizo-L only	V	V	V		V	V	
15W_CZ-L@XX	Install AMD 15W Carrizo-L only	V	V			V		
25W_CZ-L_35W_CZ@XX	Install AMD 25W Carrizo-L and Carrizo	V		V	V		V	V
PROTO@XX	Install in pre-production only	V	V	V	V			
MP@XX	Install in MP only	V				V	V	V

***Board ID by manual control

HP Restricted Secret

GPP:CZ: support GEN3 (1.05V)
CZ-L:support GEN2 (0.95V)
-->current GEN2 only.

LAN

WLAN

CARD
READER

18 PCIE_GLAN_RX_P

18 PCIE_GLAN_RX_N

23 PCIE_WLAN_RX_P

23 PCIE_WLAN_RX_N

19 PCIE_CR_RX_P

19 PCIE_CR_RX_N

U10 P_GPP_RXP[0]
U9 P_GPP_RXN[0]T6 P_GPP_RXP[1]
T5 P_GPP_RXN[1]T9 P_GPP_RXP[2]
T8 P_GPP_RXN[2]P7 P_GPP_RXP[3]
P6 P_GPP_RXN[3]

VDDP

R312 CZ-L@1.69K/F 4 P_ZVDDP

Carrizo : 196 ohm
Carrizo-L: 1.69 K
R312 CS21692FB01
CZ@196/F_4

P_GFX(4:7)_RXP(N) : Only Carrizo

P10 P_GFX_RXP[0]
P9 P_GFX_RXN[0]N8 P_GFX_RXP[1]
N7 P_GFX_RXN[1]N9 P_GFX_RXP[2]
N8 P_GFX_RXN[2]L7 P_GFX_RXP[3]
L6 P_GFX_RXN[3]L10 P_GFX_RXP[4]
L9 P_GFX_RXN[4]K6 P_GFX_RXP[5]
K5 P_GFX_RXN[5]K9 P_GFX_RXP[6]
K8 P_GFX_RXN[6]J7 P_GFX_RXP[7]
J6 P_GFX_RXN[7]

U6B

PCIE

P_GPP_TXP[0]
P_GPP_TXN[0]P_GPP_TXP[1]
P_GPP_TXN[1]P_GPP_TXP[2]
P_GPP_TXN[2]P_GPP_TXP[3]
P_GPP_TXN[3]

P_ZVSS/P_RX_ZVDDP

M2 P_GFX_TXP[0]
M1 P_GFX_TXN[0]L1 P_GFX_TXP[1]
L0 P_GFX_TXN[1]L4 P_GFX_TXP[2]
L3 P_GFX_TXN[2]J1 P_GFX_TXP[3]
J0 P_GFX_TXN[3]J4 P_GFX_TXP[4]
J3 P_GFX_TXN[4]H2 P_GFX_TXP[5]
H1 P_GFX_TXN[5]G1 P_GFX_TXP[6]
G0 P_GFX_TXN[6]G4 P_GFX_TXP[7]
G3 P_GFX_TXN[7]R1 PCIE_TXP0_C
R2 PCIE_TXN0_CR4 PCIE_TXP1_C
R3 PCIE_TXN1_CN1 PCIE_TXP2_C
N2 PCIE_TXN2_CN4 PCIE_TXP3_C
N3 PCIE_TXN3_C

P_RX_ZVDDP

M2 P_GFX_TXP[0]
M1 P_GFX_TXN[0]L1 P_GFX_TXP[1]
L0 P_GFX_TXN[1]L4 P_GFX_TXP[2]
L3 P_GFX_TXN[2]J1 P_GFX_TXP[3]
J0 P_GFX_TXN[3]J4 P_GFX_TXP[4]
J3 P_GFX_TXN[4]H2 P_GFX_TXP[5]
H1 P_GFX_TXN[5]G1 P_GFX_TXP[6]
G0 P_GFX_TXN[6]G4 P_GFX_TXP[7]
G3 P_GFX_TXN[7]C34 0.1U/10V/X5R_4
C36 0.1U/10V/X5R_4C29 0.1U/10V/X5R_4
C30 0.1U/10V/X5R_4C28 0.1U/10V/X5R_4
C27 0.1U/10V/X5R_4C28 0.1U/10V/X5R_4
C27 0.1U/10V/X5R_4PCIE_GLAN_TX_P
PCIE_GLAN_TX_NPCIE_WLAN_TX_P
PCIE_WLAN_TX_NPCIE_CR_TX_P
PCIE_CR_TX_N

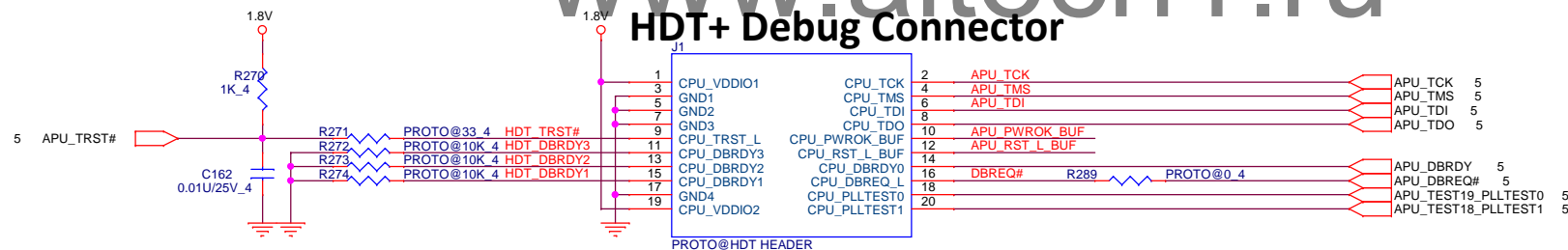
Cdep : 220 nF for CZ(if need
support GEN3) and 100nF for
Gen2

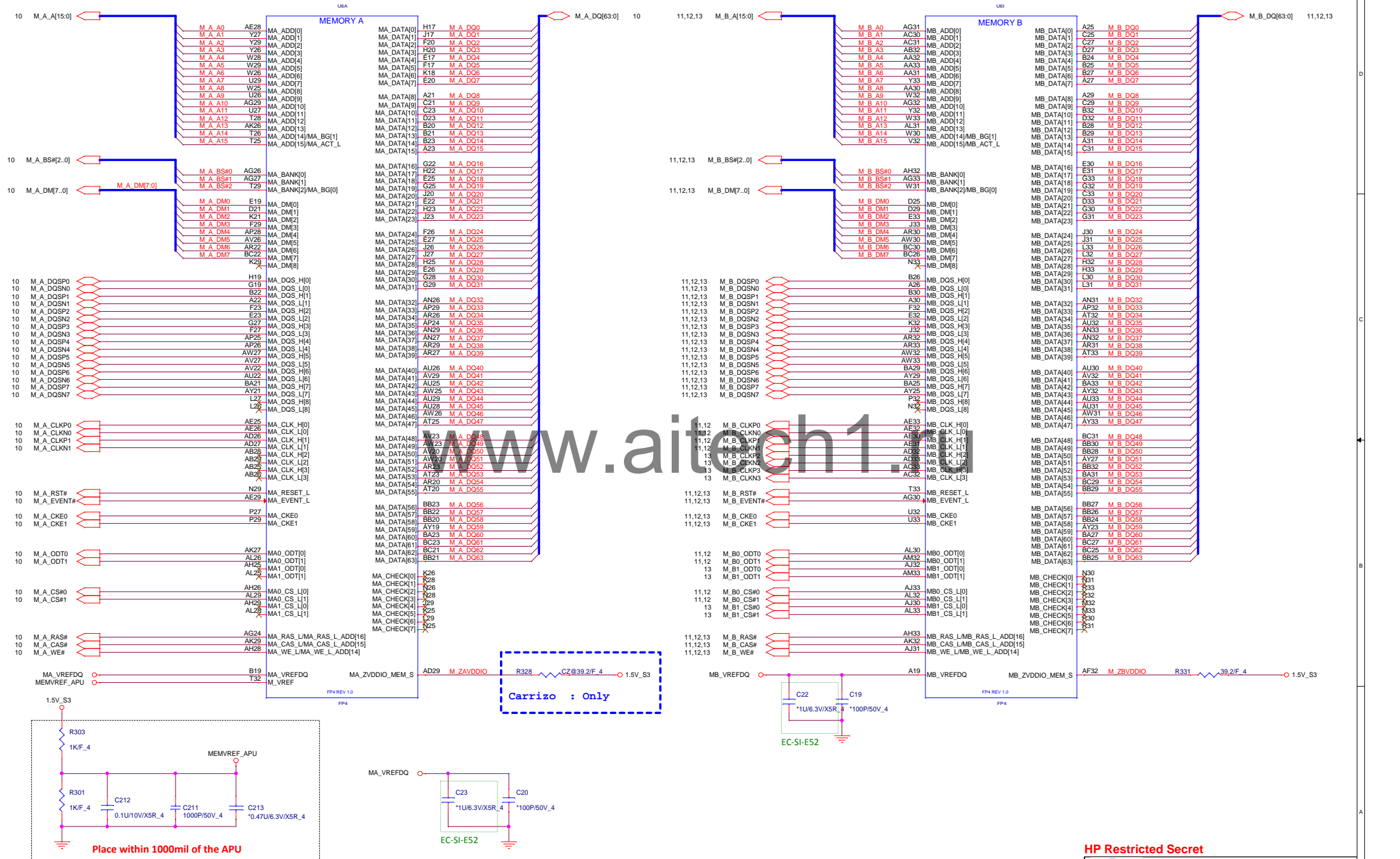
R309 CZ-L@1K/F 4 VDDP

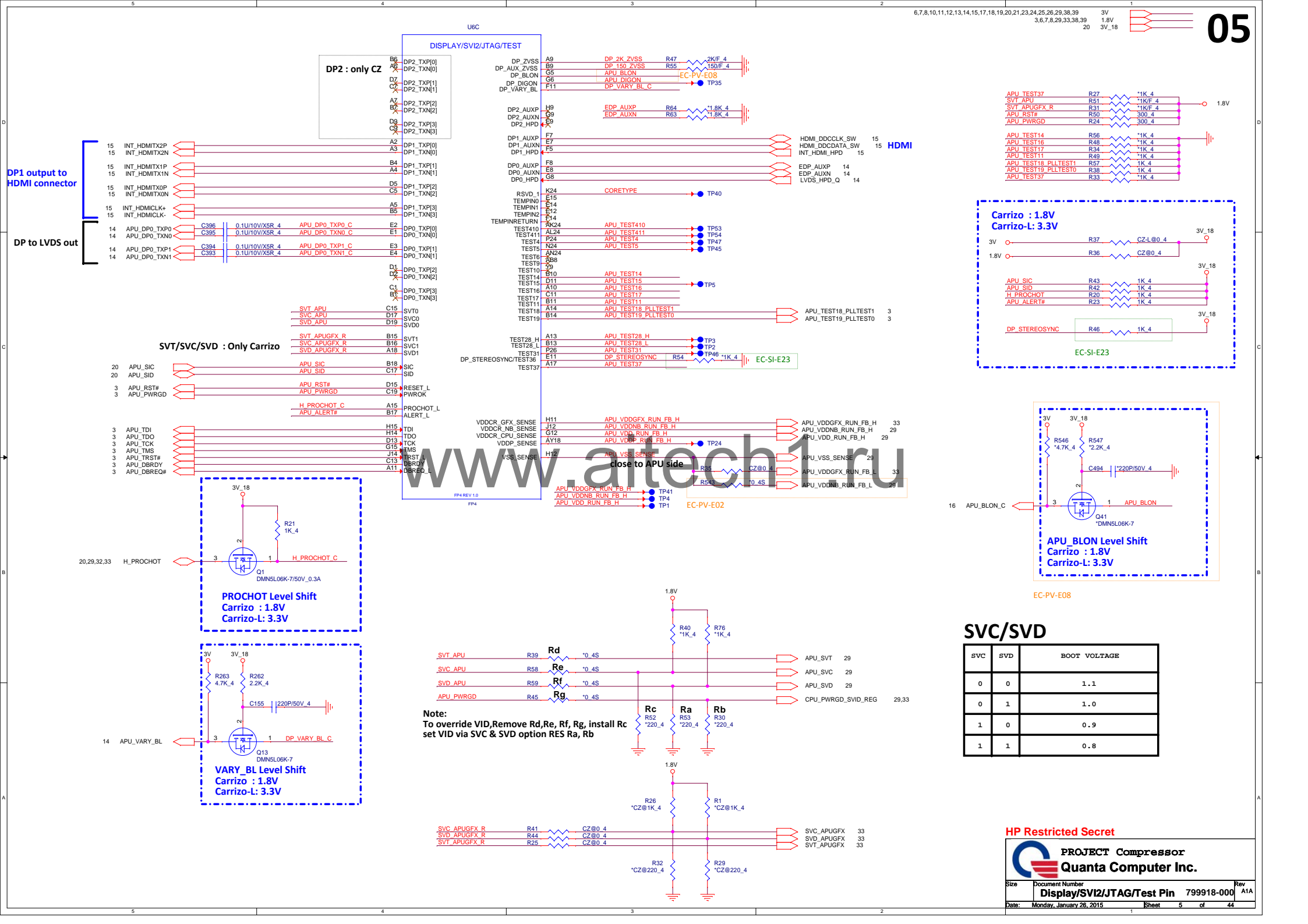
Carrizo : 196 ohm pull down
Carrizo-L : 1K Pull up

P_GFX(4:7)_TXP(N) : Only Carrizo

www.aitech1.ru
HDT+ Debug Connector



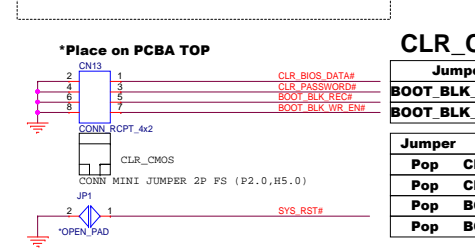
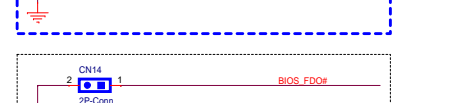
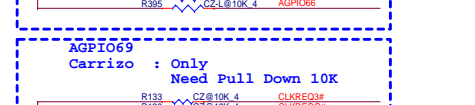
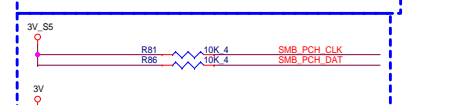
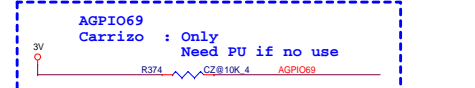
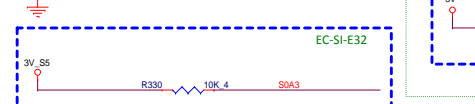
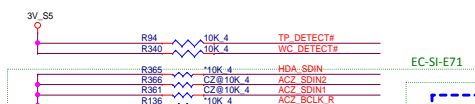
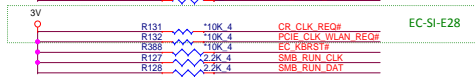
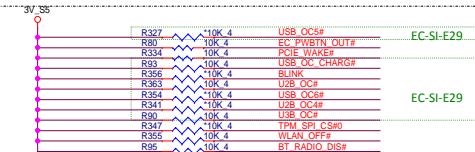




NC,no install by default



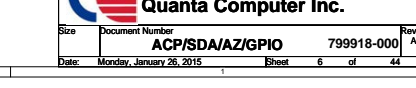
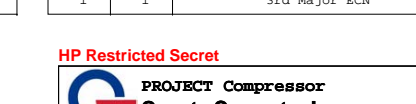
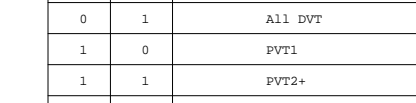
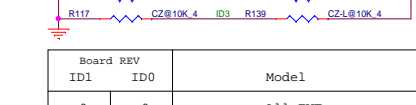
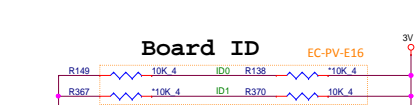
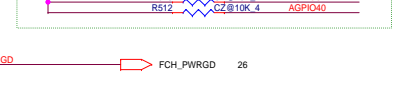
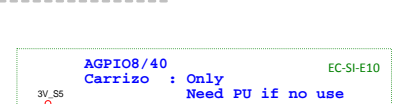
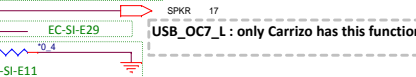
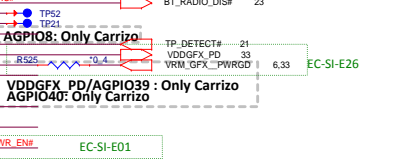
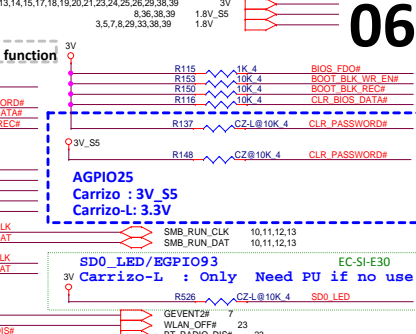
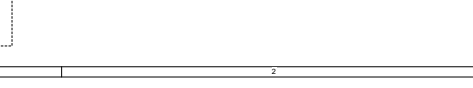
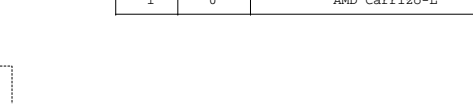
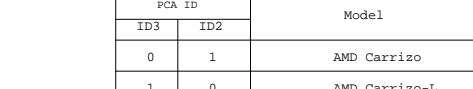
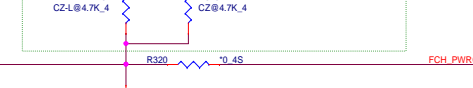
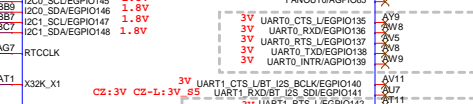
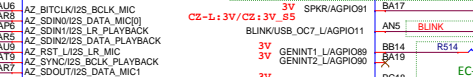
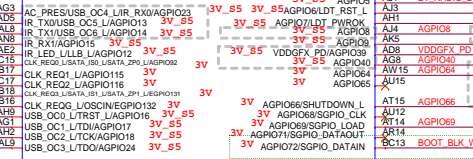
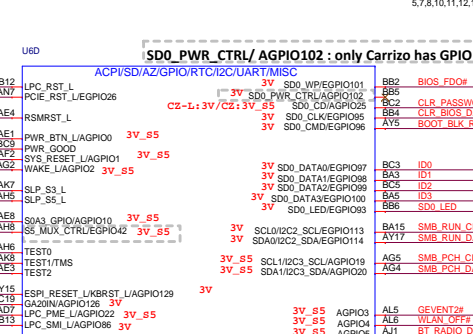
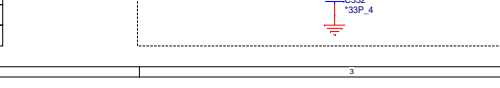
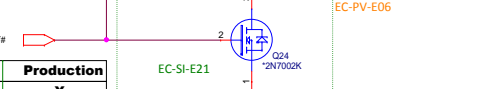
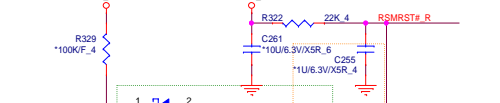
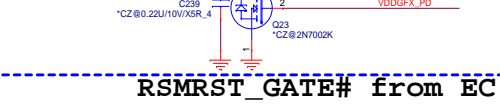
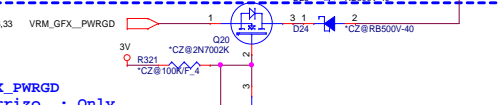
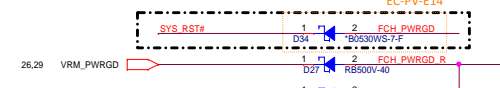
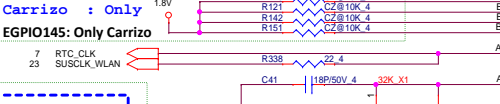
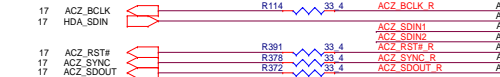
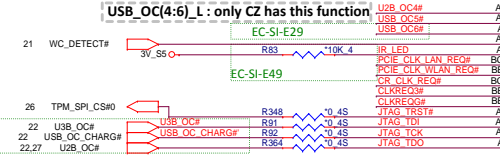
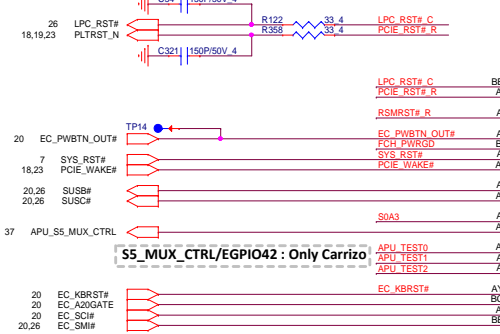
TEST2	TEST1	TEST0	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-FCH pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH JTAG can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



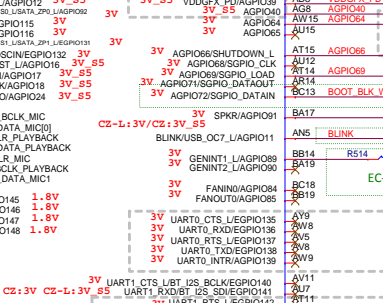
CLR_CMOS

Jumper	Pre-production	Production
BOOT_BLK_Recovery	X	X
BOOT_BLK_Enable	O	X

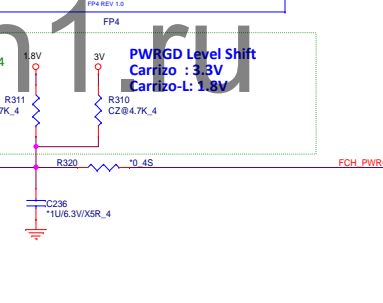
Jumper	Type
Pop CLR BIOS DAT	
Pop CLR PASSWD	
Pop BOOT_BLK_Recovery	
Pop BOOT_BLK_Enable	



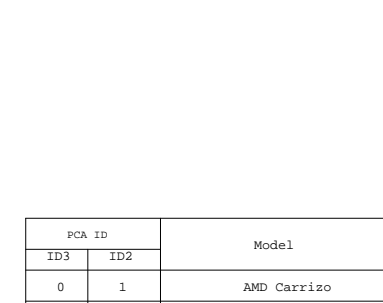
SD0_PWR_CTRL/ AGPIO102 : only Carrizo has GPIO function



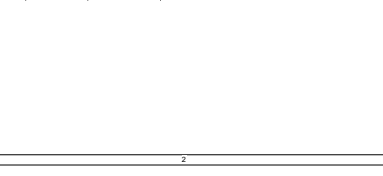
AGPIO102 : only Carrizo has GPIO function



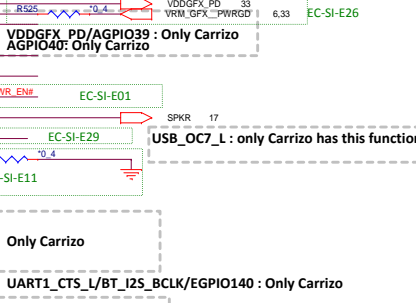
AGPIO102 : only Carrizo has GPIO function



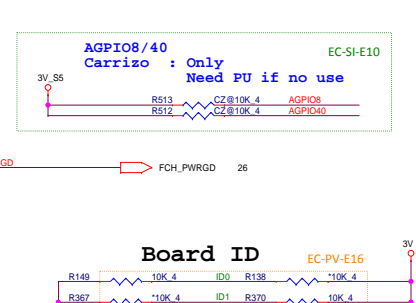
AGPIO102 : only Carrizo has GPIO function



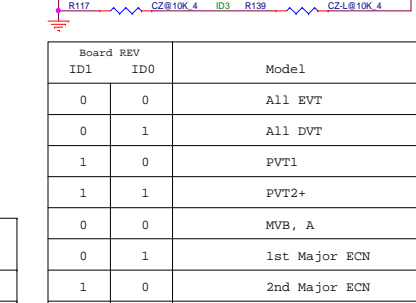
AGPIO102 : only Carrizo has GPIO function



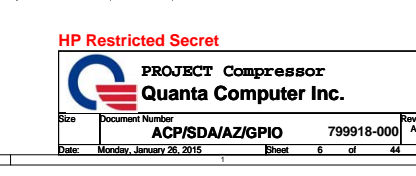
AGPIO102 : only Carrizo has GPIO function



AGPIO102 : only Carrizo has GPIO function



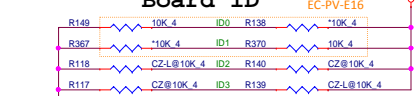
AGPIO102 : only Carrizo has GPIO function



PCA ID

ID3	ID2	Model
0	1	AMD Carrizo
1	0	AMD Carrizo-L

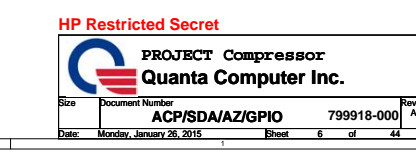
Board ID



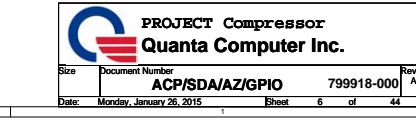
Board ID

Board REV	ID1	ID0	Model
0	0	0	All EVT
0	0	1	All DVT
1	0	0	PVT1
1	0	1	PVT2+
0	0	0	MVB, A
0	1	1	1st Major ECN
1	0	0	2nd Major ECN
1	1	1	3rd Major ECN

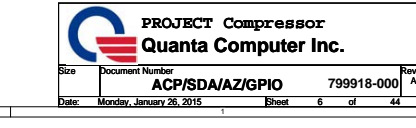
Board ID



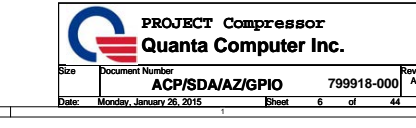
Board ID



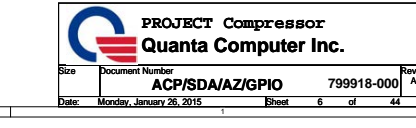
Board ID



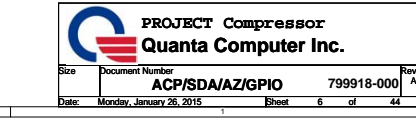
Board ID



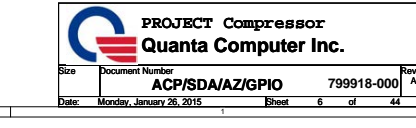
Board ID



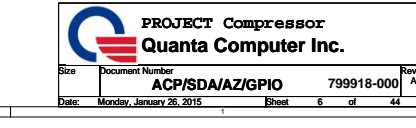
Board ID



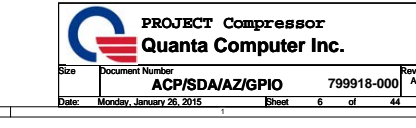
Board ID



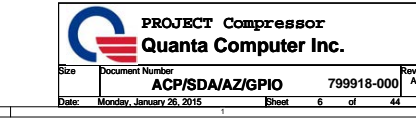
Board ID



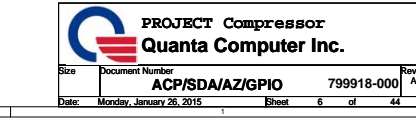
Board ID



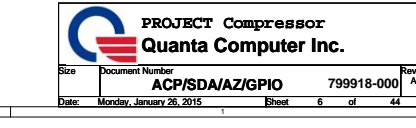
Board ID



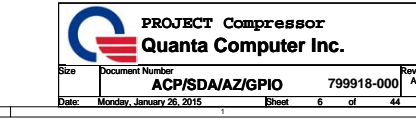
Board ID



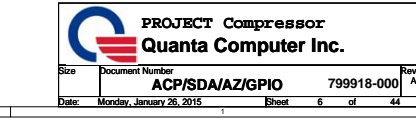
Board ID



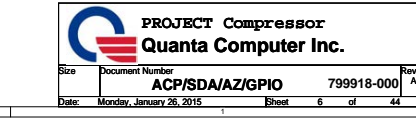
Board ID



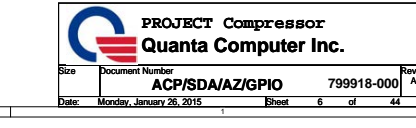
Board ID



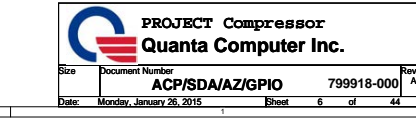
Board ID



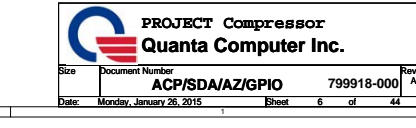
Board ID



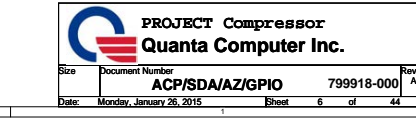
Board ID



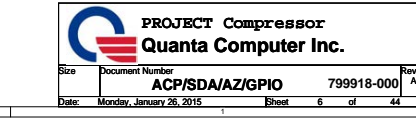
Board ID



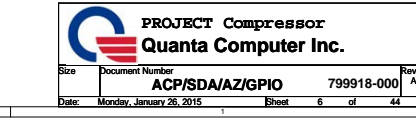
Board ID



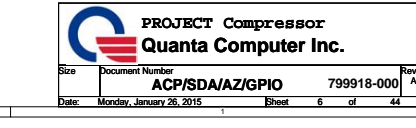
Board ID



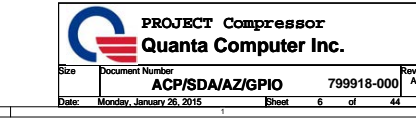
Board ID



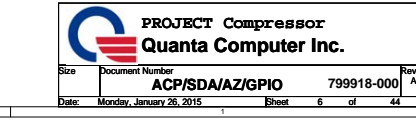
Board ID



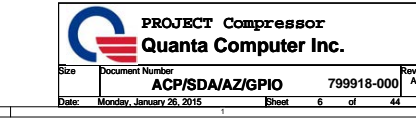
Board ID



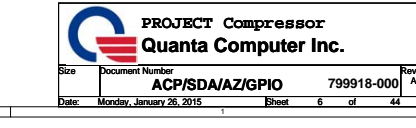
Board ID



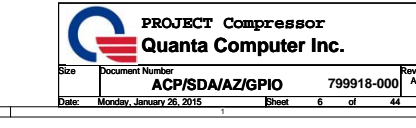
Board ID



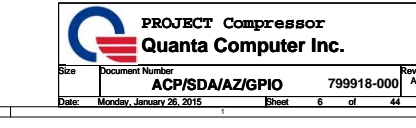
Board ID



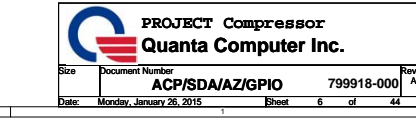
Board ID



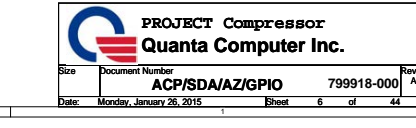
Board ID



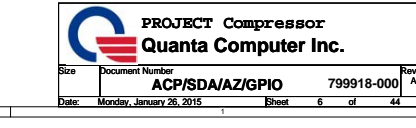
Board ID



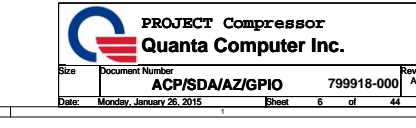
Board ID



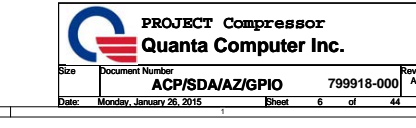
Board ID



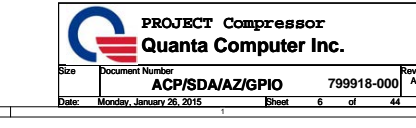
Board ID



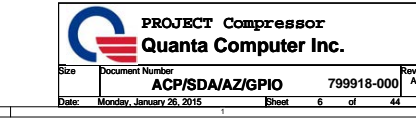
Board ID



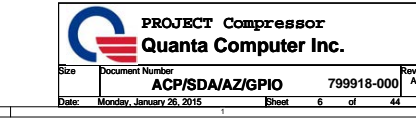
Board ID



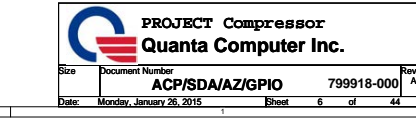
Board ID



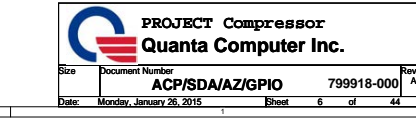
Board ID



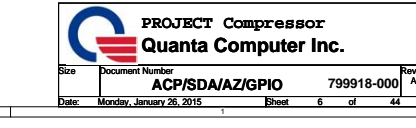
Board ID



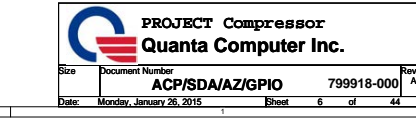
Board ID



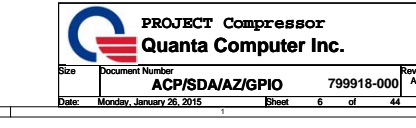
Board ID



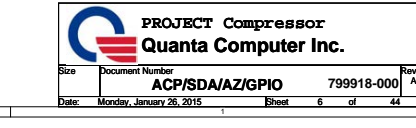
Board ID



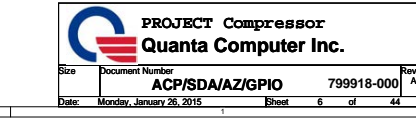
Board ID



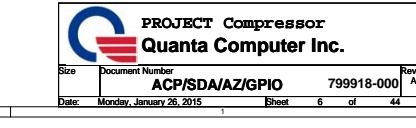
Board ID



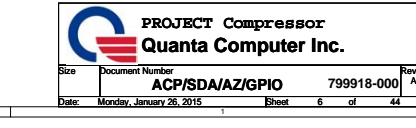
Board ID



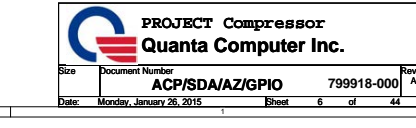
Board ID



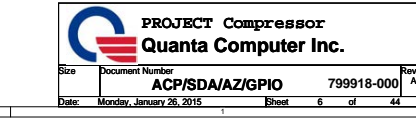
Board ID



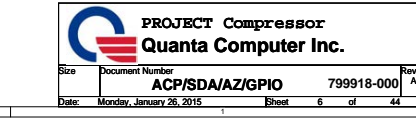
Board ID



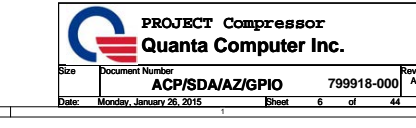
Board ID



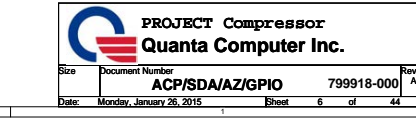
Board ID



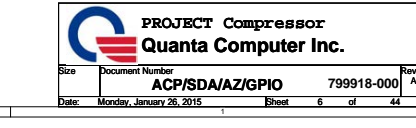
Board ID



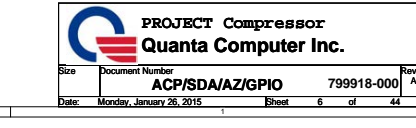
Board ID



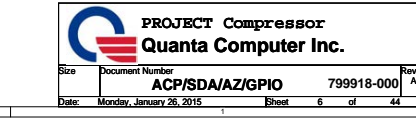
Board ID



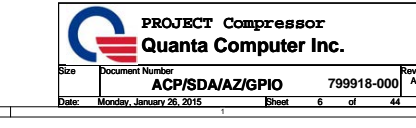
Board ID



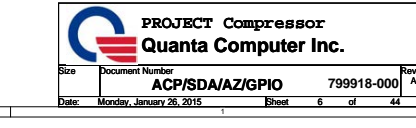
Board ID



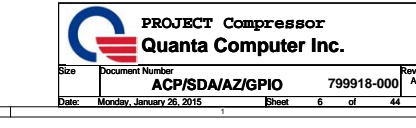
Board ID



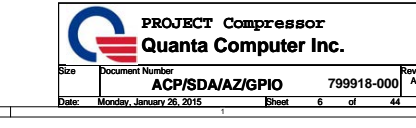
Board ID



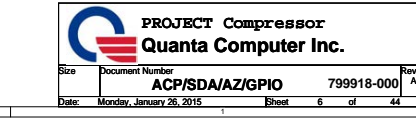
Board ID



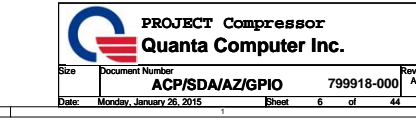
Board ID



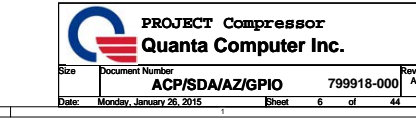
Board ID



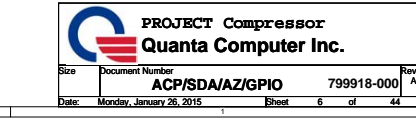
Board ID



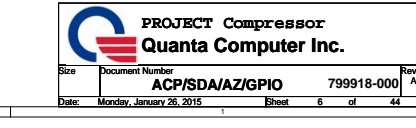
Board ID



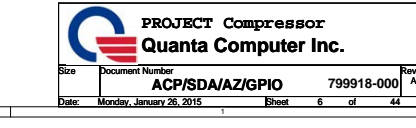
Board ID



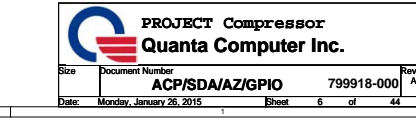
Board ID

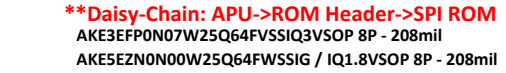


Board ID



Board ID

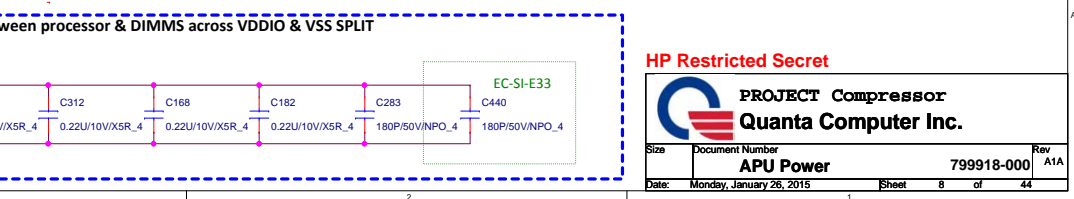
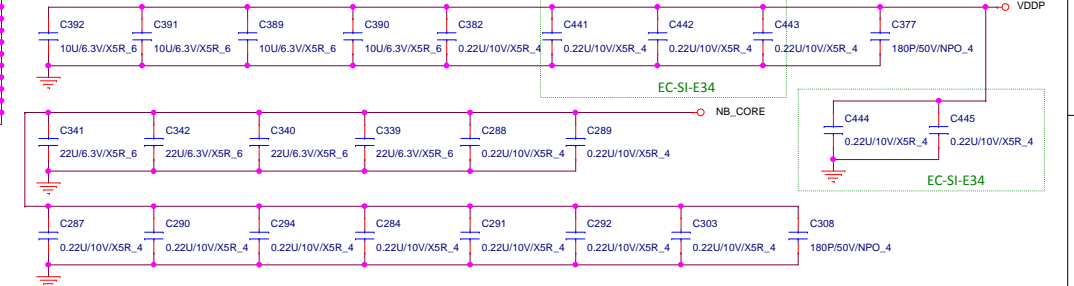
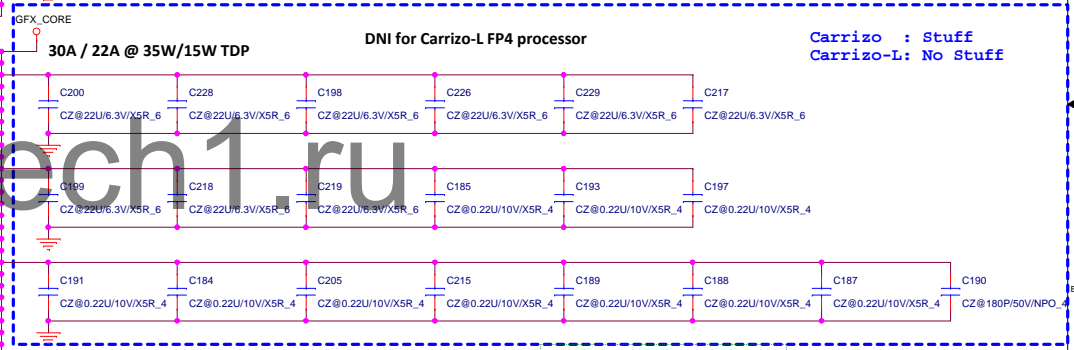
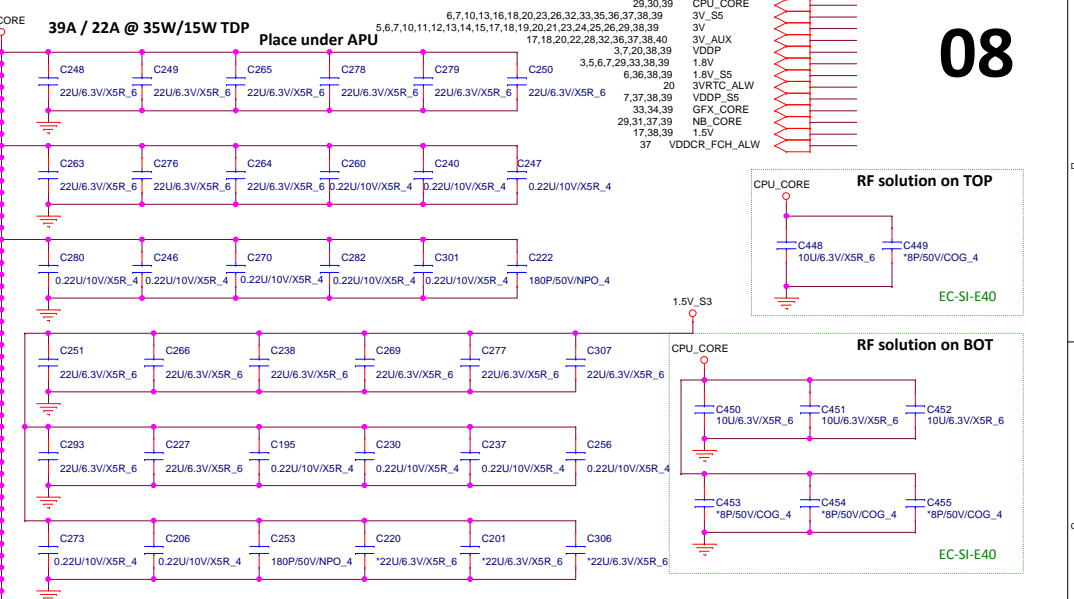
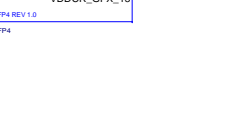
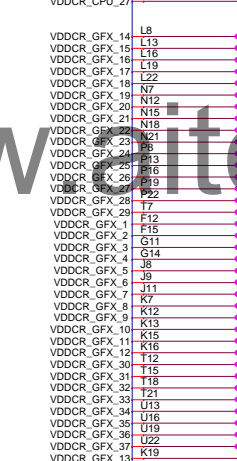
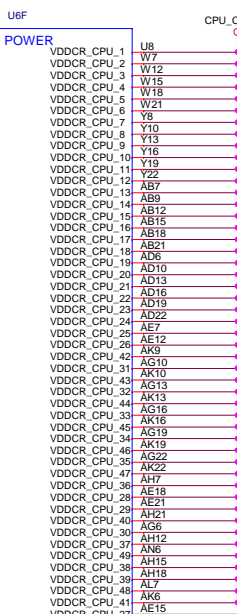
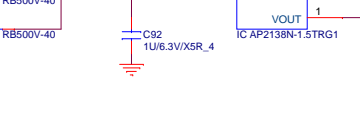
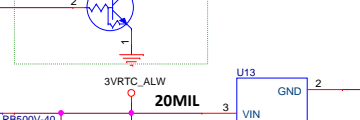
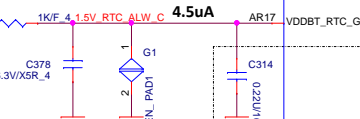
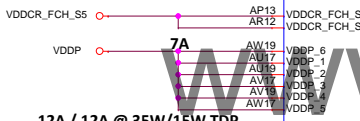
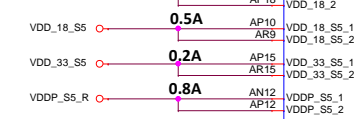
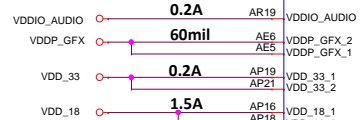
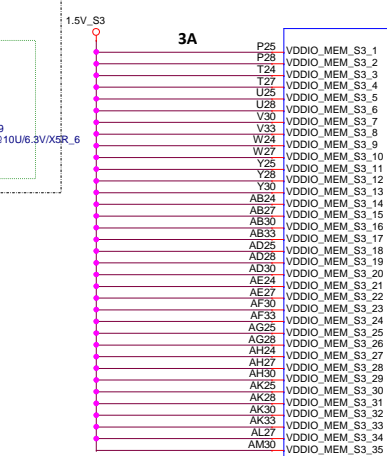
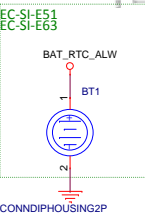
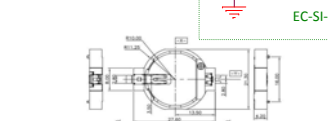
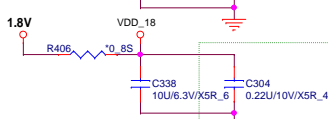
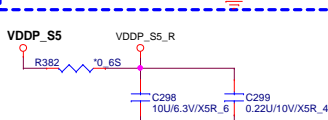
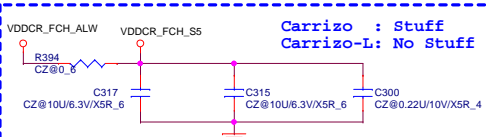
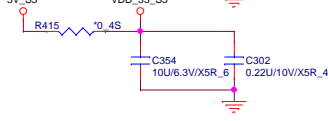
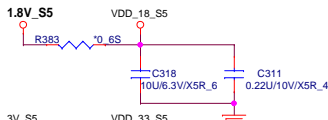
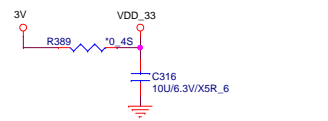
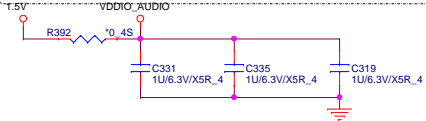
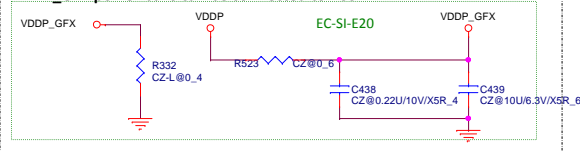




REQUIRED STRAPS

	CK_33M_EC	LPC_CLK1	LFRAME#	RTC_CLK	GEVENT2#		SYS_RST#
PULL HIGH	BOOT Fail Timer ENABLE	Internal CLKGEN ENABLE	SPI ROM	Normal Power Timing ENABLE	CZ-L SPI Voltage 1.8V	Enhanced Reset logic for faster resume from S5 DEFAULT	normal reset mode DEFAULT
		DEFAULT	DEFAULT	DEFAULT			
PULL LOW	BOOT Fail Timer DISABLE DEFAULT	Internal CLKGEN DISABLE	LPC ROM	Normal Power Timing DISABLE	SPI Voltage 3.3V DEFAULT	Traditional Reset logic	short reset mode

If P_GFX [7:0] are not used,
VDDP_GFX power balls can be connected to VSS .



08

RF solution on TOP

EC-SI-E40

RF solution on BOT

Carrizo • Stuff

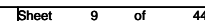
Carrizo-L: No Stuff

HP Restricted Secret



PROJECT Compressor
Quanta Computer Inc.

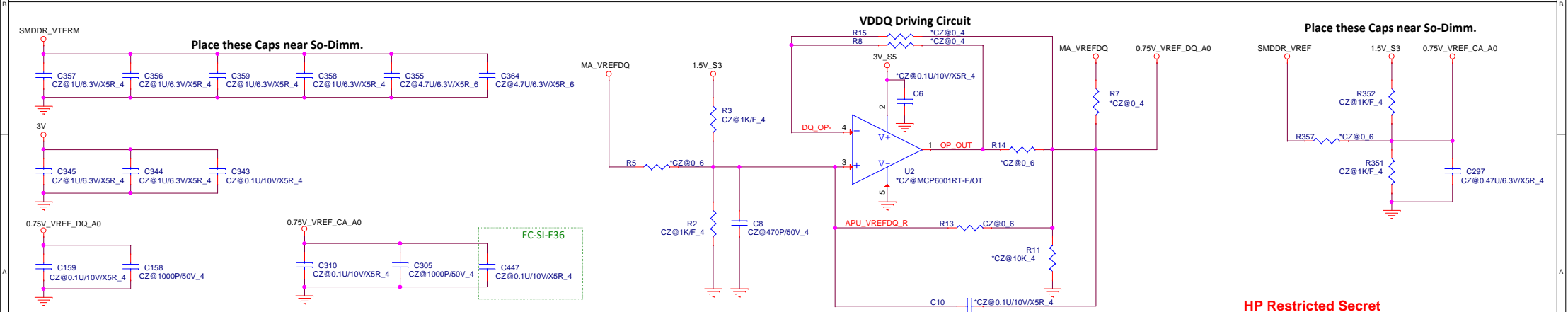
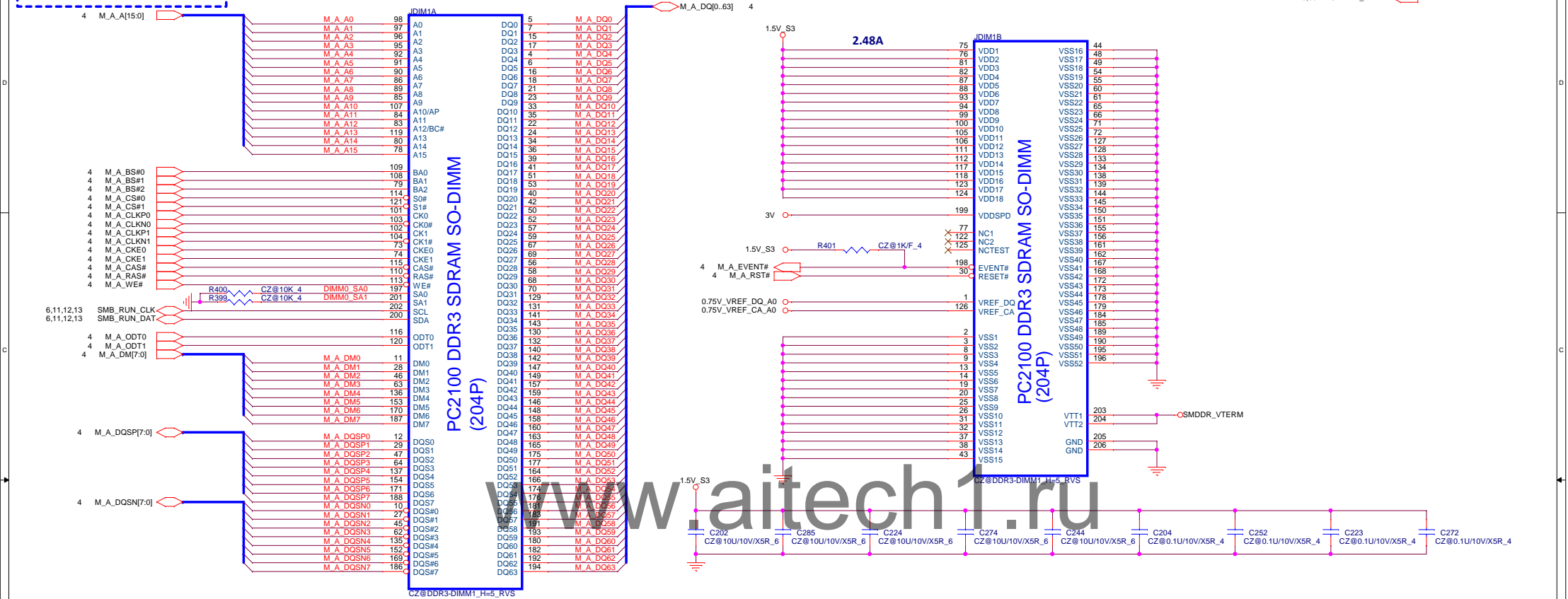
Size	Document Number	Rev
	APU Power	799918-000
Date:	Monday, January 26, 2015	Sheet 8 of 44



DDR_RVS(DDR)

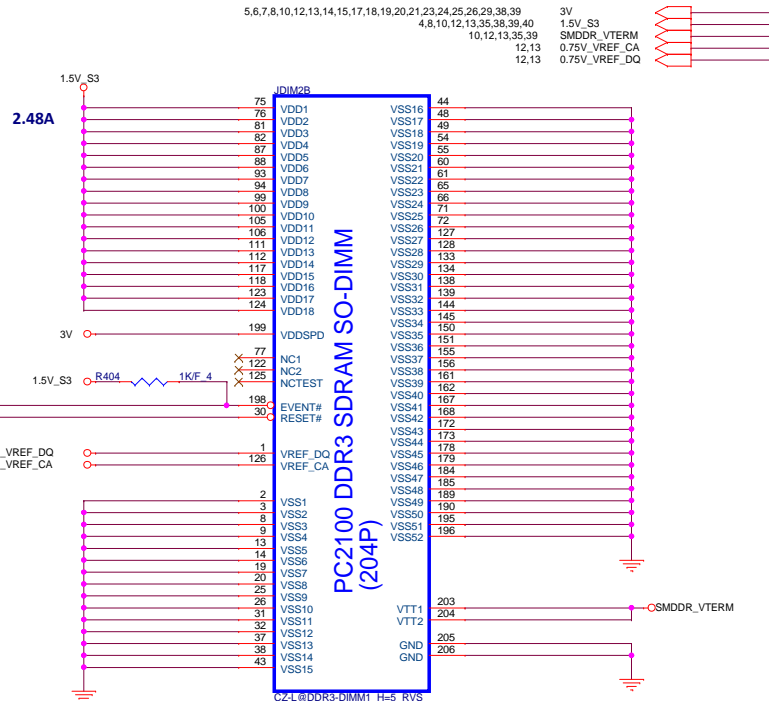
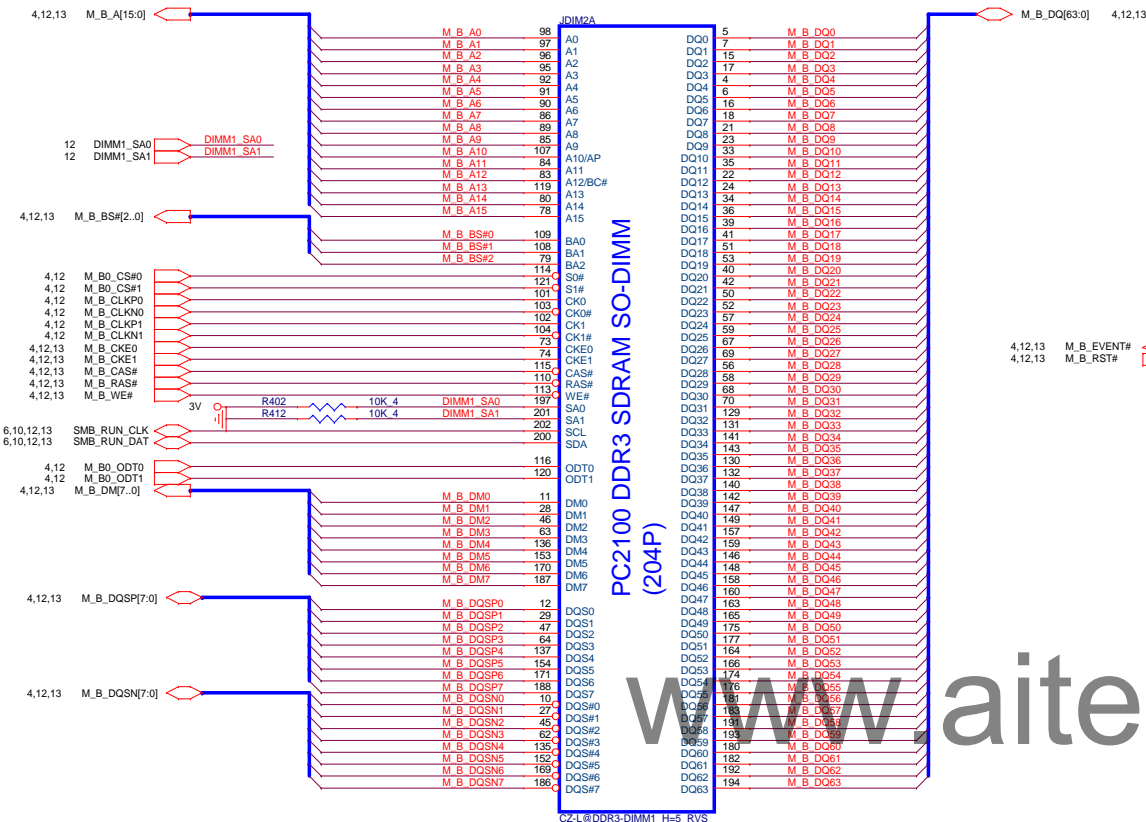
Carriizo : Only

10



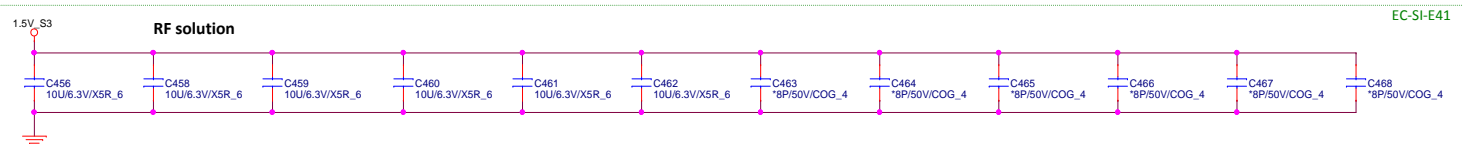
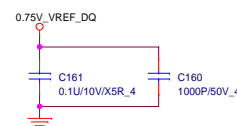
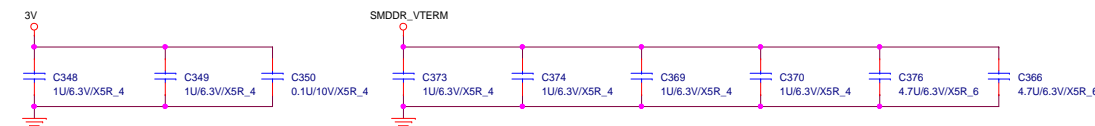
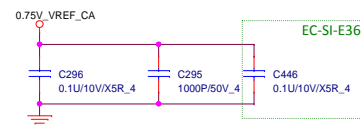
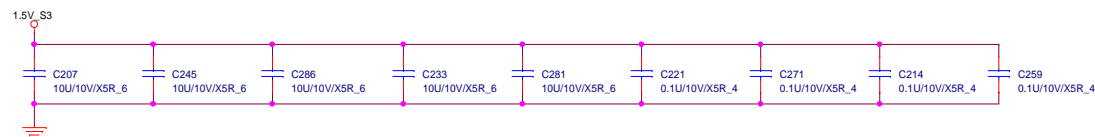
HP Restricted Secret

DDR_RVS(DDR)



11

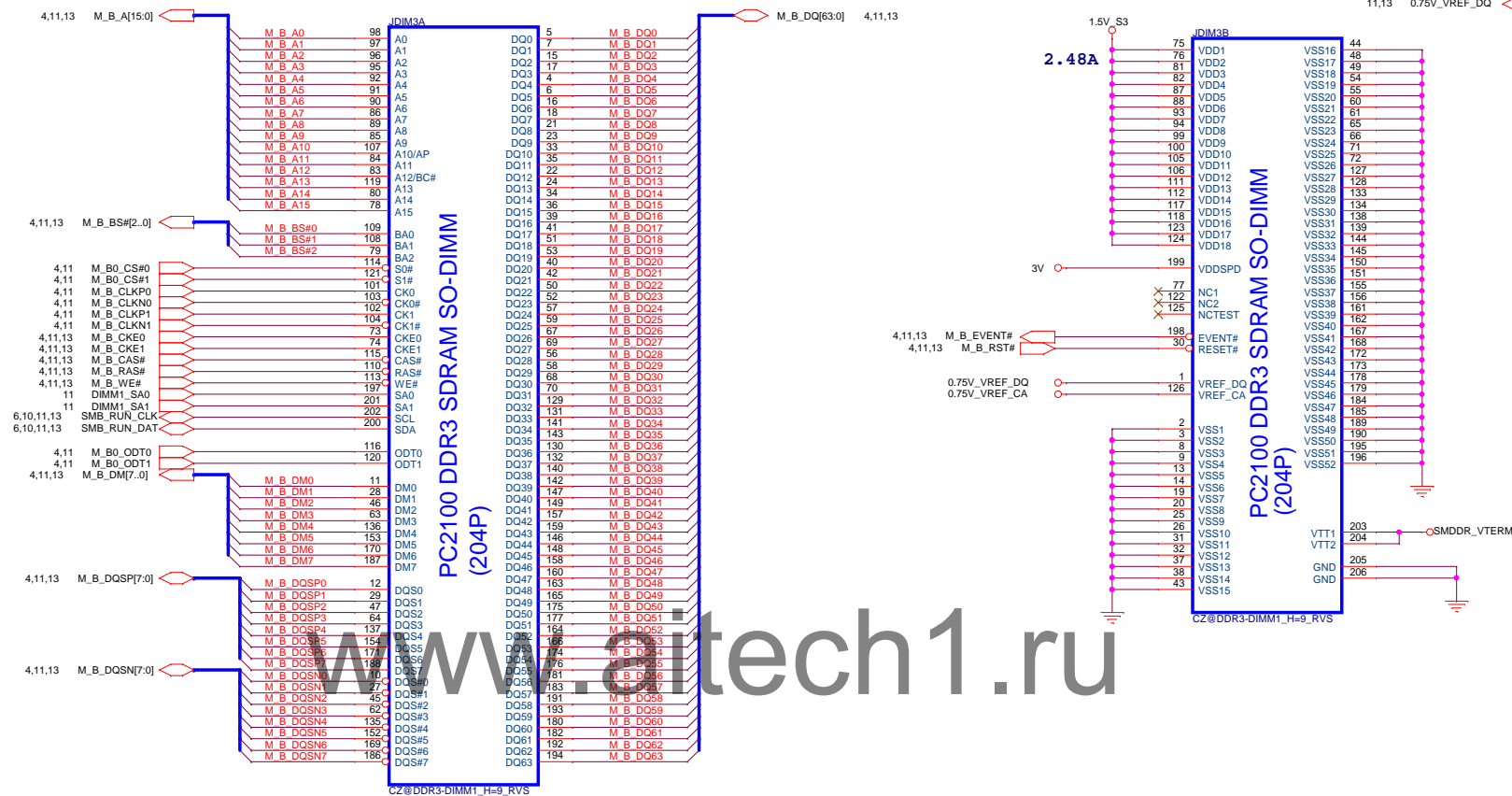
Place these Caps near So-Dimm.




HP Restricted Secret

Carrizo : Only

12



 PROJECT Compressor Quanta Computer Inc.			
Size	Document Number		Rev
	Carrizo DDR3 DIMM-2 (H=9.2)	799918-000	A1A
Date:	Monday, January 26, 2015	Sheet 12 of 44	

Carrizo-L : Only



Place these Caps near So-Dimm.

SMDR_VTERM

3V

0.75V_VREF_DQ

0.75V_VREF_CA

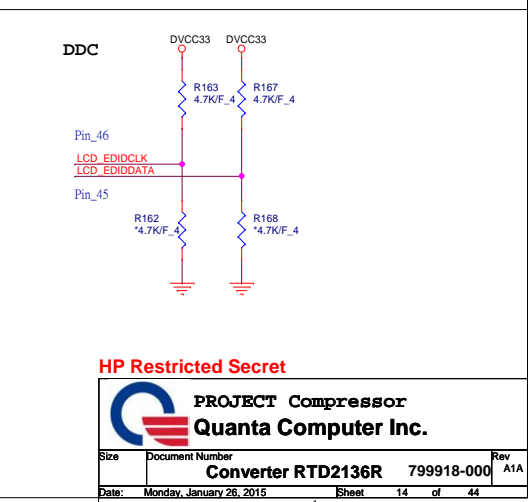
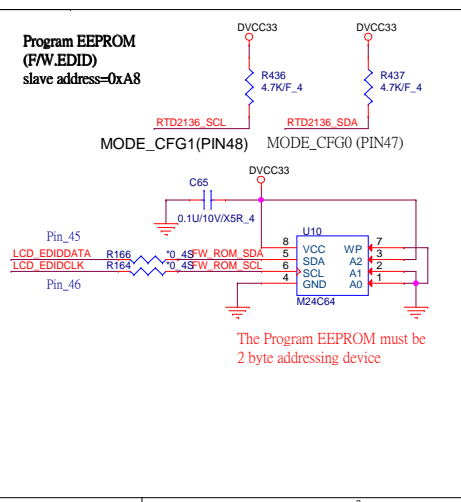
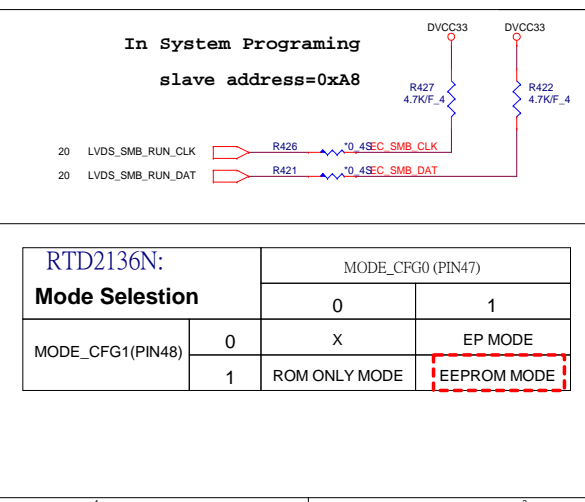
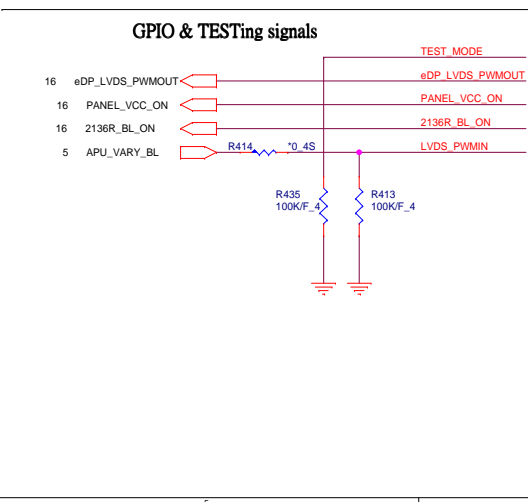
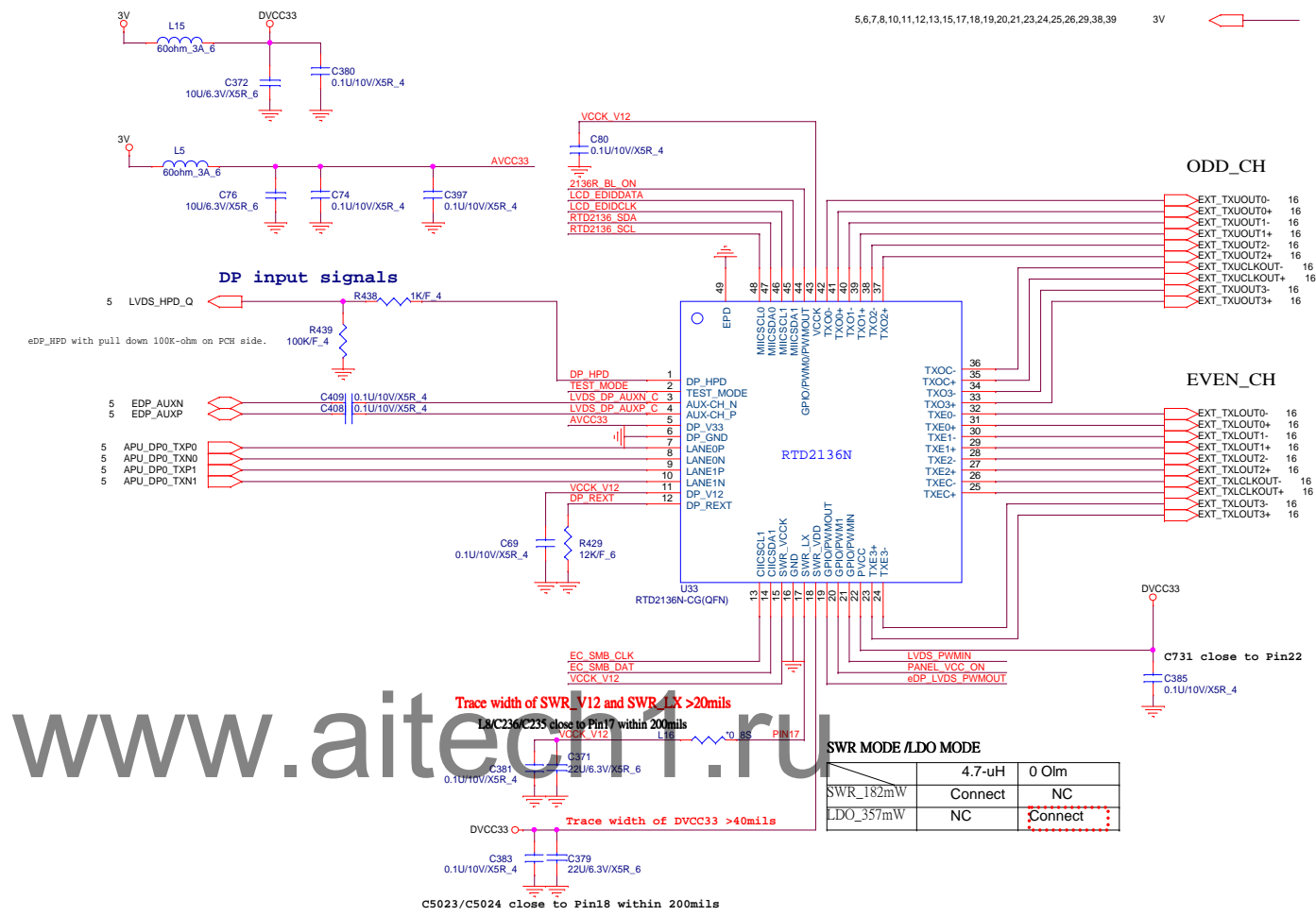
MB_VREF

Capacitor values and labels:

- C360: CZ-L@1U/6.3V/X5R_4
- C363: CZ-L@1U/6.3V/X5R_4
- C361: CZ-L@1U/6.3V/X5R_4
- C362: CZ-L@1U/6.3V/X5R_4
- C367: CZ-L@4.7U/6.3V/X5R_6
- C368: CZ-L@4.7U/6.3V/X5R_6
- C353: CZ-L@1U/6.3V/X5R_4
- C352: CZ-L@1U/6.3V/X5R_4
- C351: CZ-L@0.1U/10V/X5R_4
- C157: CZ-L@0.1U/10V/X5R_4
- C156: CZ-L@1000P/50V_4
- C313: CZ-L@0.1U/10V/X5R_4
- C309: CZ-L@1000P/50V_4



Size	Document Number	Rev
	Carrizo-L DDR3 DIMM-1 (H=9.2) 799918-000	A1A
Date:	Monday, January 26, 2015	Sheet 13 of 44



15



The diagram shows a 5V regulator circuit. A 0.1µF capacitor (labeled D10 RB500V40) is connected in parallel with the input. A 220Ω resistor (labeled R228) is connected in series with the load. The output is labeled 5V. The text "EMI (EMC)" is written below the diagram.

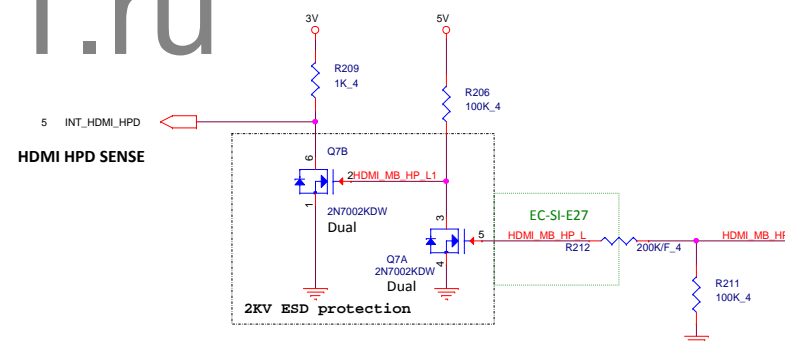



Timing diagram for EC-Si-E42 showing the following signals and their rising edges:

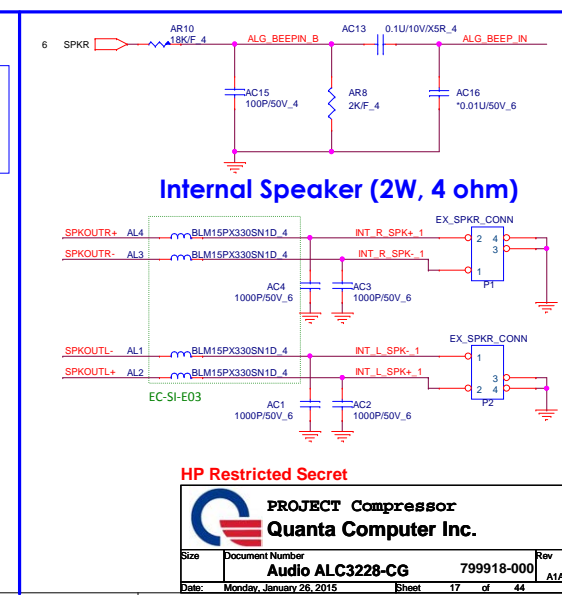
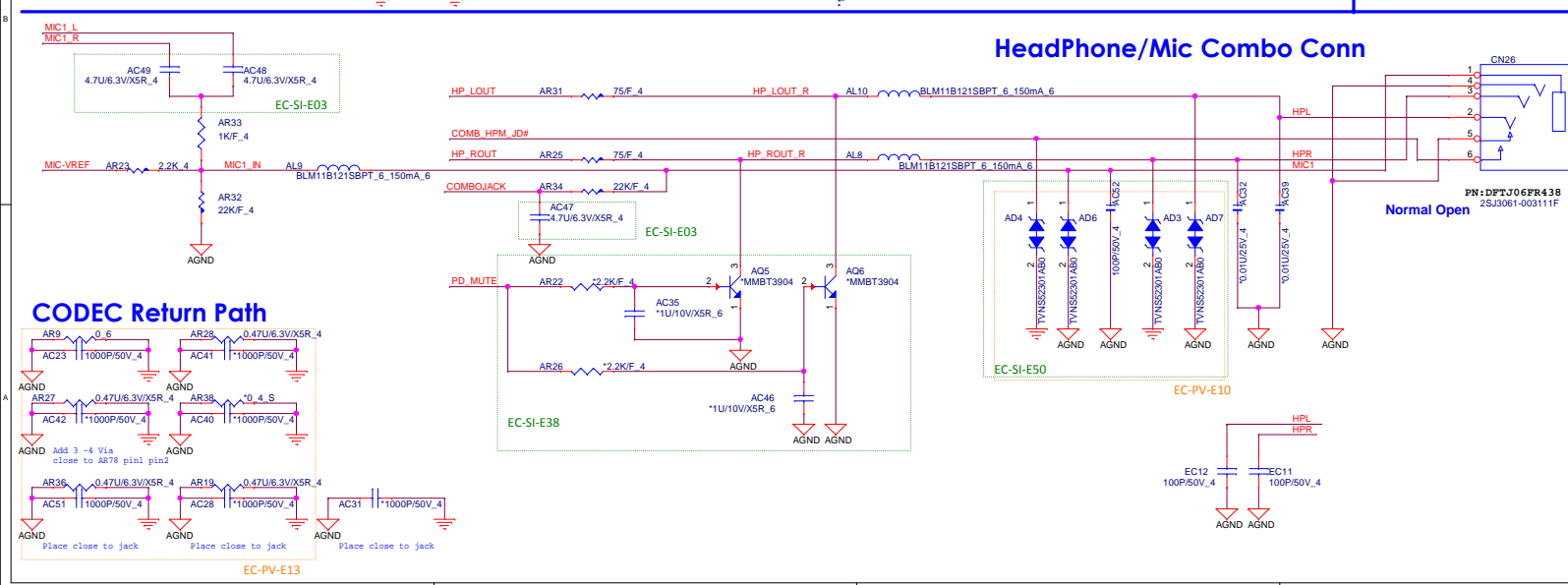
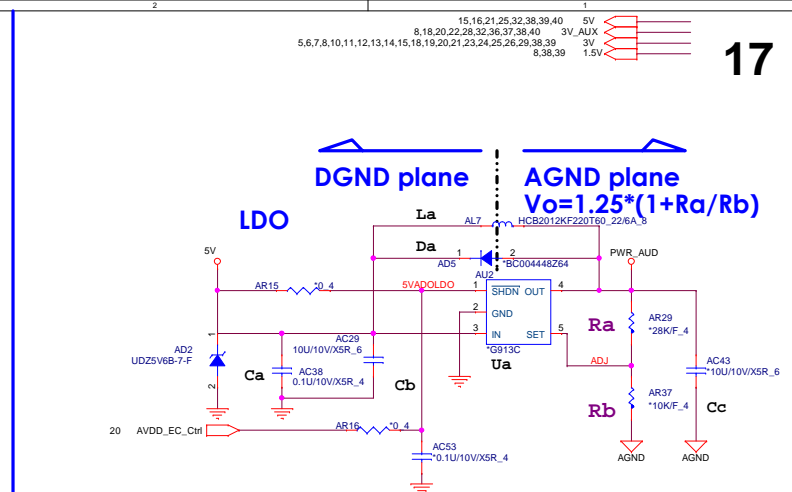
- INT_HDMITX2P_C (Rising edge labeled R188 120/F 4)
- INT_HDMITX2N_C (Rising edge labeled R188 120/F 4)
- INT_HDMITX1P_C (Rising edge labeled R188 120/F 4)
- INT_HDMITX1N_C (Rising edge labeled R188 120/F 4)
- INT_HDMITX0P_C (Rising edge labeled R202 120/F 4)
- INT_HDMITX0N_C (Rising edge labeled R202 120/F 4)
- INT_HDMICKL+_CONN (Rising edge labeled R203 120/F 4)
- INT_HDMICKL-_CONN (Rising edge labeled R203 120/F 4)

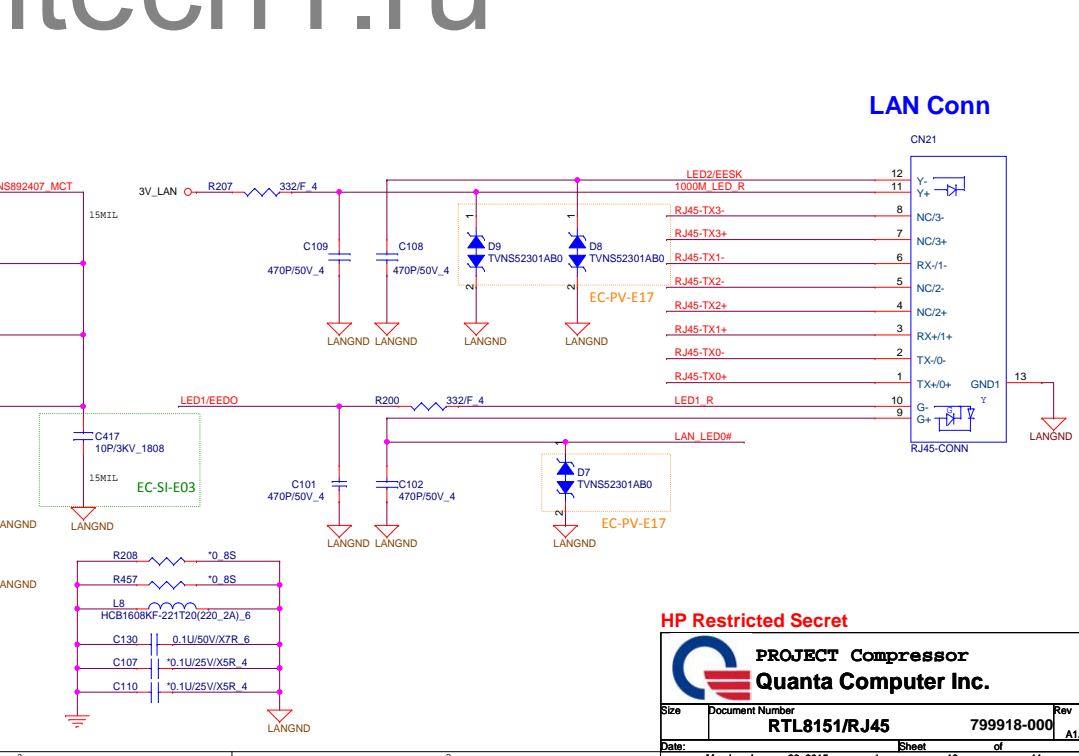
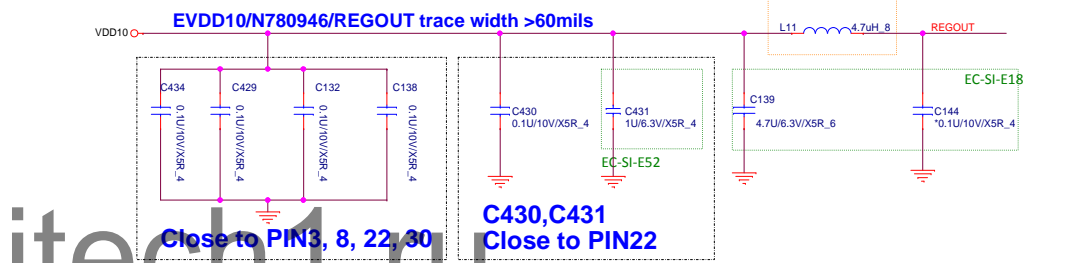
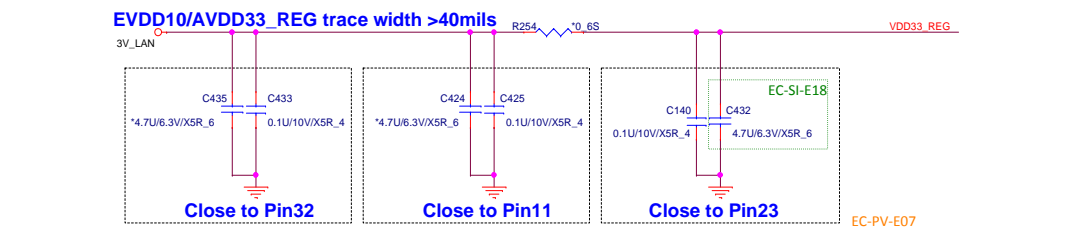
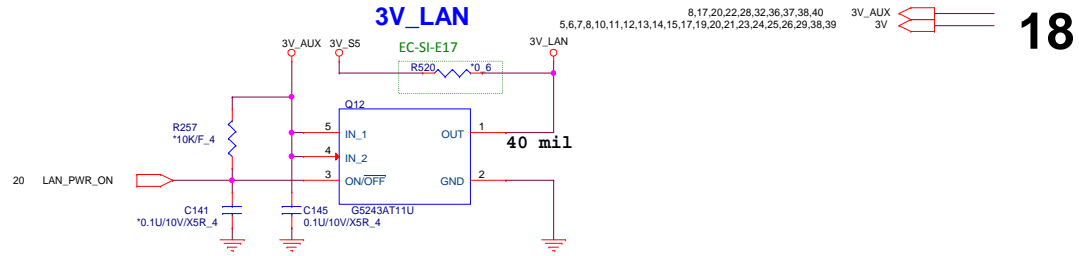
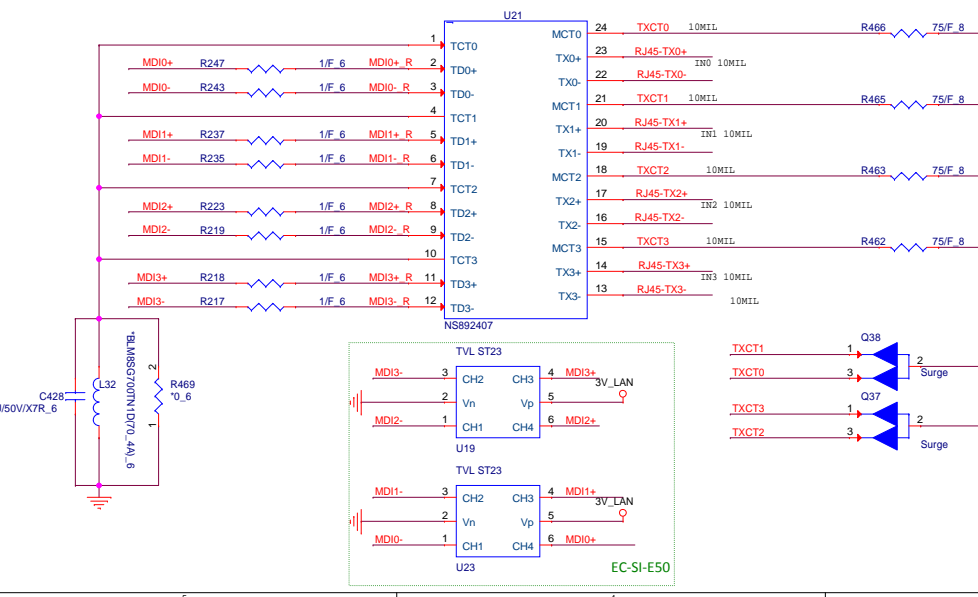
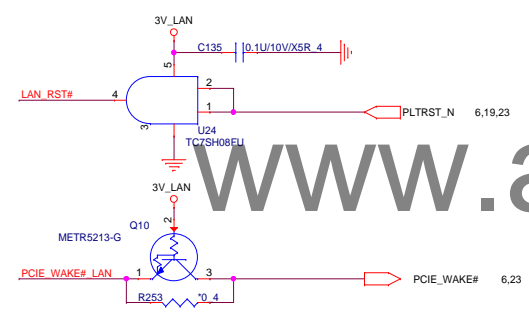
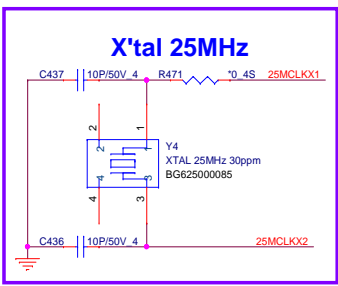
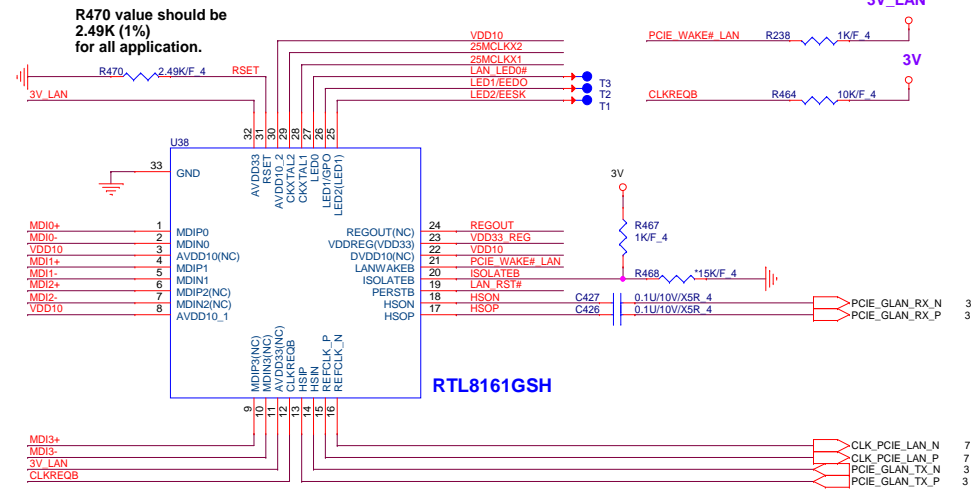
EC-Si-E42

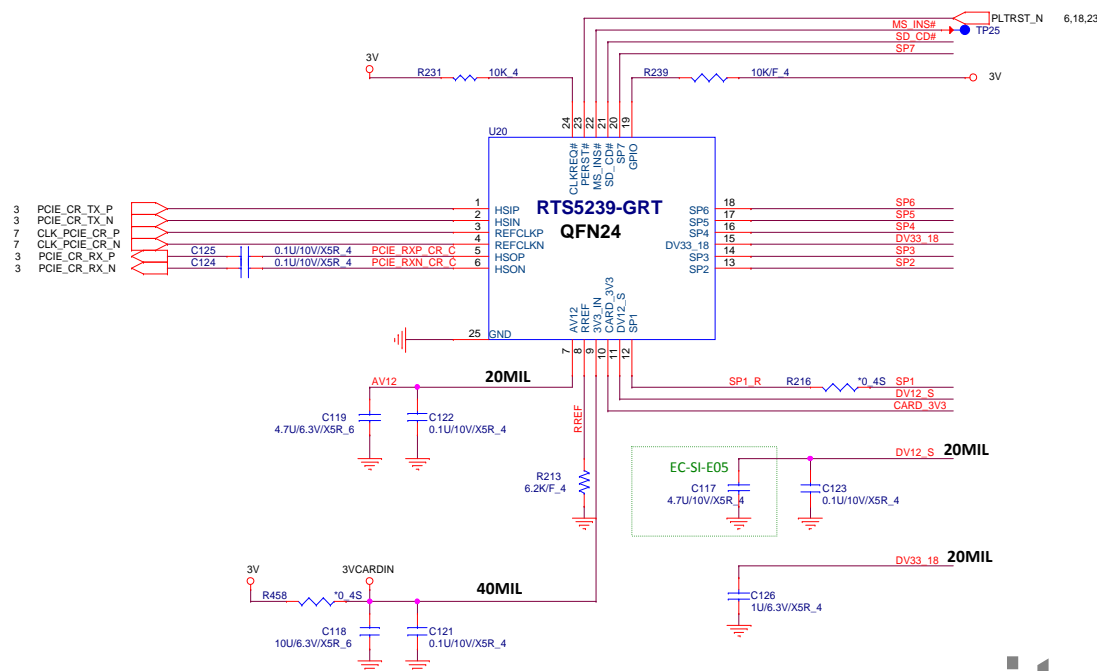
HDMI HPD SENSE



 PROJECT Compressor Quanta Computer Inc.		Rev
Size	Document Number	A
	HDMI	799918-000
Date:	Monday, January 26, 2015	Sheet 15 of 44





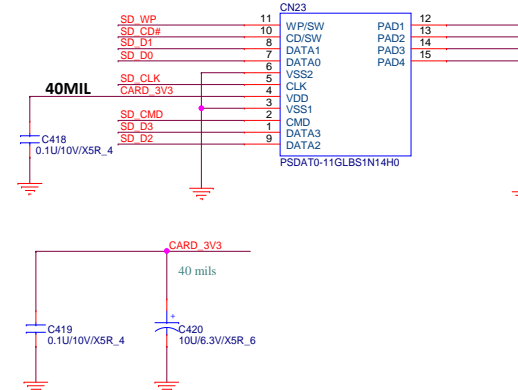


Place close to U20

SP1	R461	33 4	SD D1
SP2	R460	33 4	SD D0
SP3	R459	33 4	SD CLK
SP4	R220	33 4	SD CMD
SP5	R227	33 4	SD D3
SP6	R234	33 4	SD D2
SP7	R240	33 4	SD WP

SD D1	C423	5.6P/16V_4
SD D0	C422	5.6P/16V_4
SD CLK	C421	5.6P/16V_4
SD D3	C127	5.6P/16V_4
SD D2	C129	5.6P/16V_4

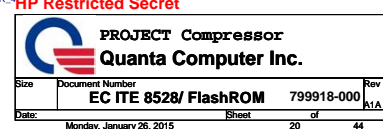
SD connector



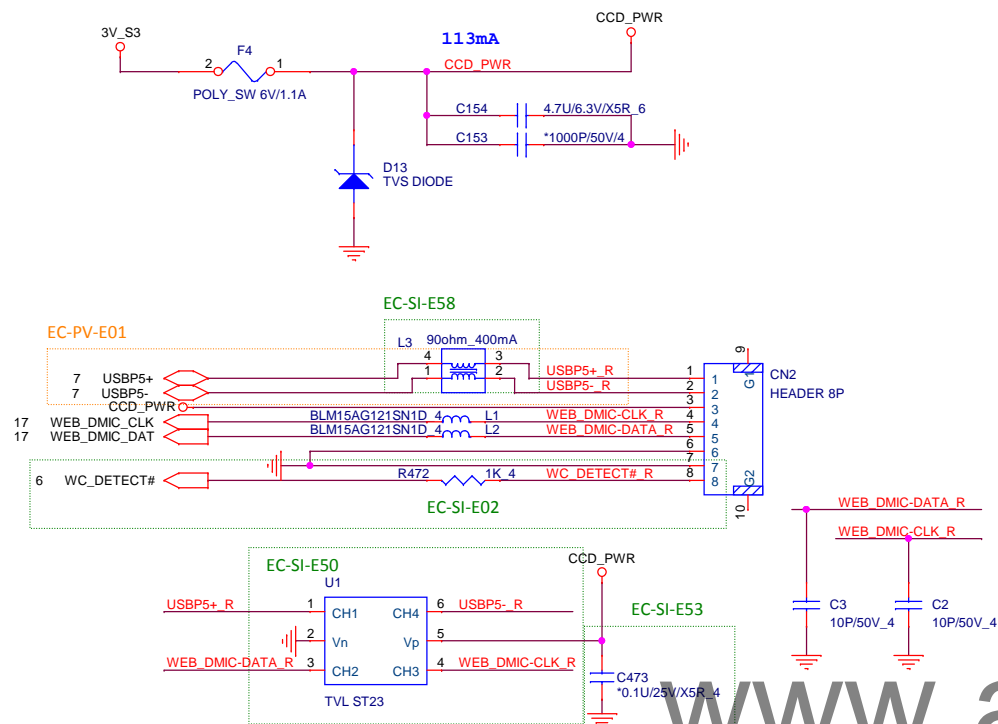
PIN NO.	SD NAME
P1	DAT3
P2	CMD
P3	VSS
P4	VDD
P5	CLK
P6	VSS
P7	DAT0
P8	DAT1
P9	DAT2
P10	C/D SW Pin
P11	W/P SW Pin

www.aitech1.ru

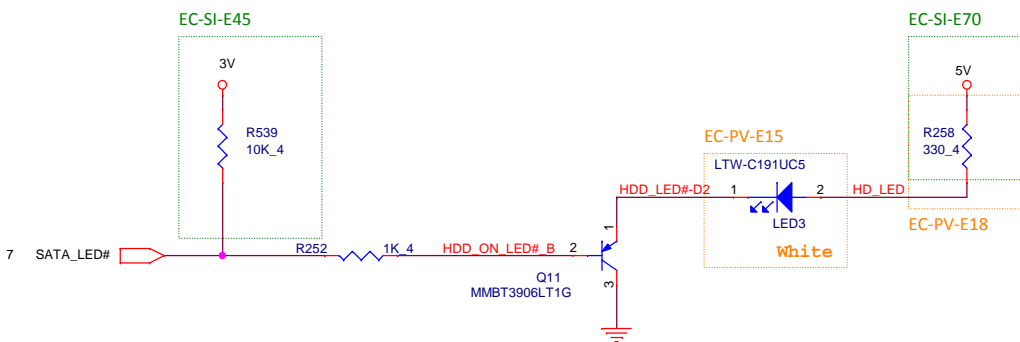
HP Restricted Secret



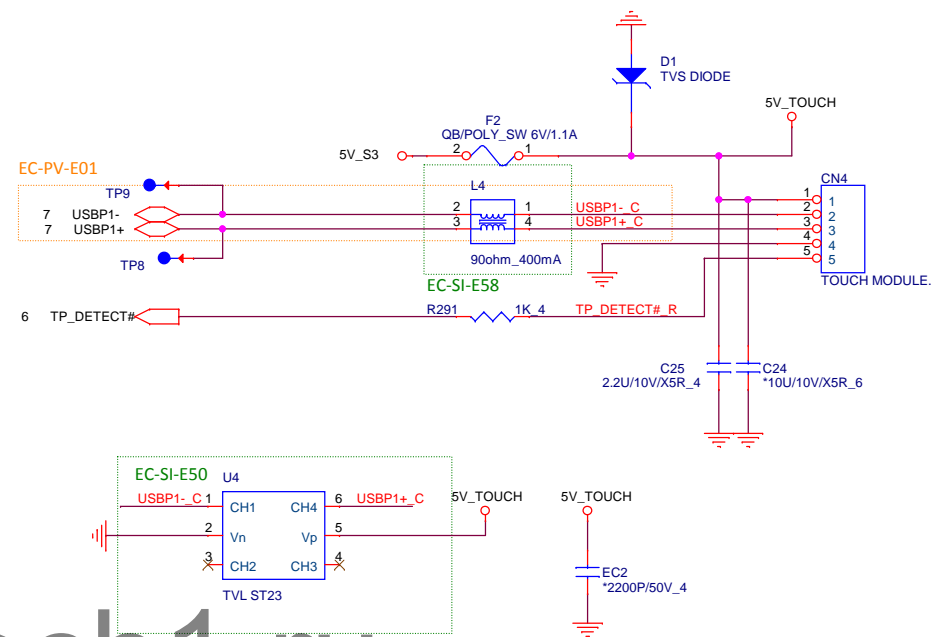
WEBCAM



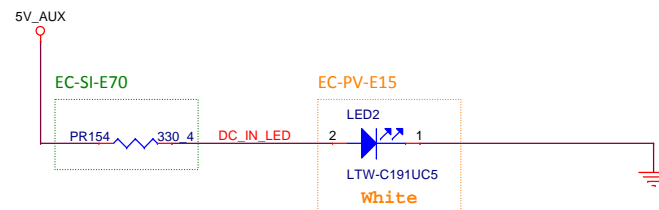
SATA LED



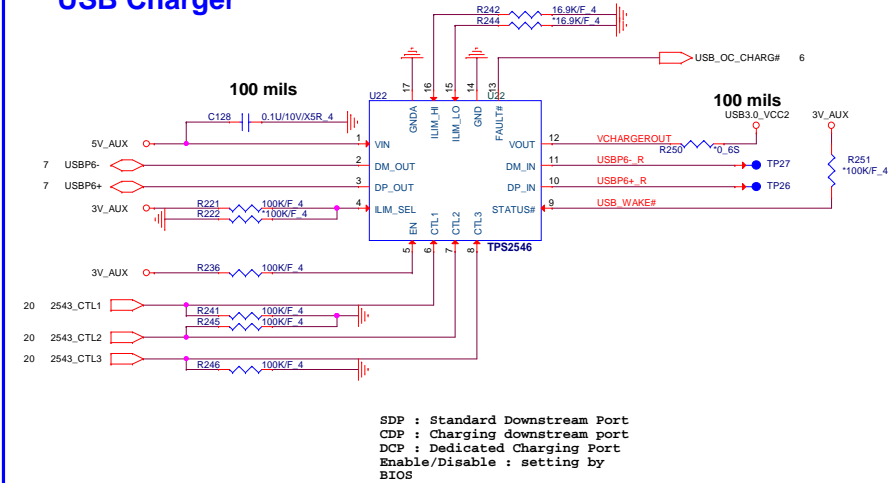
Touch Panel



DC-IN LED



HP Restricted Secret




pins: www.aitech1.ru

The diagram shows the pinout for component U34, labeled "U34" and "TW DF10 04 AD1". It is a 10-pin connector. The pins are numbered 1 through 10. The connections are as follows:

- Pins 1 and 2: USBP0- R
- Pins 3 and 4: USBP0+ R
- Pins 5 and 6: GND_3/8
- Pins 7 and 8: USBP3- R
- Pins 9 and 10: USBP3+ R

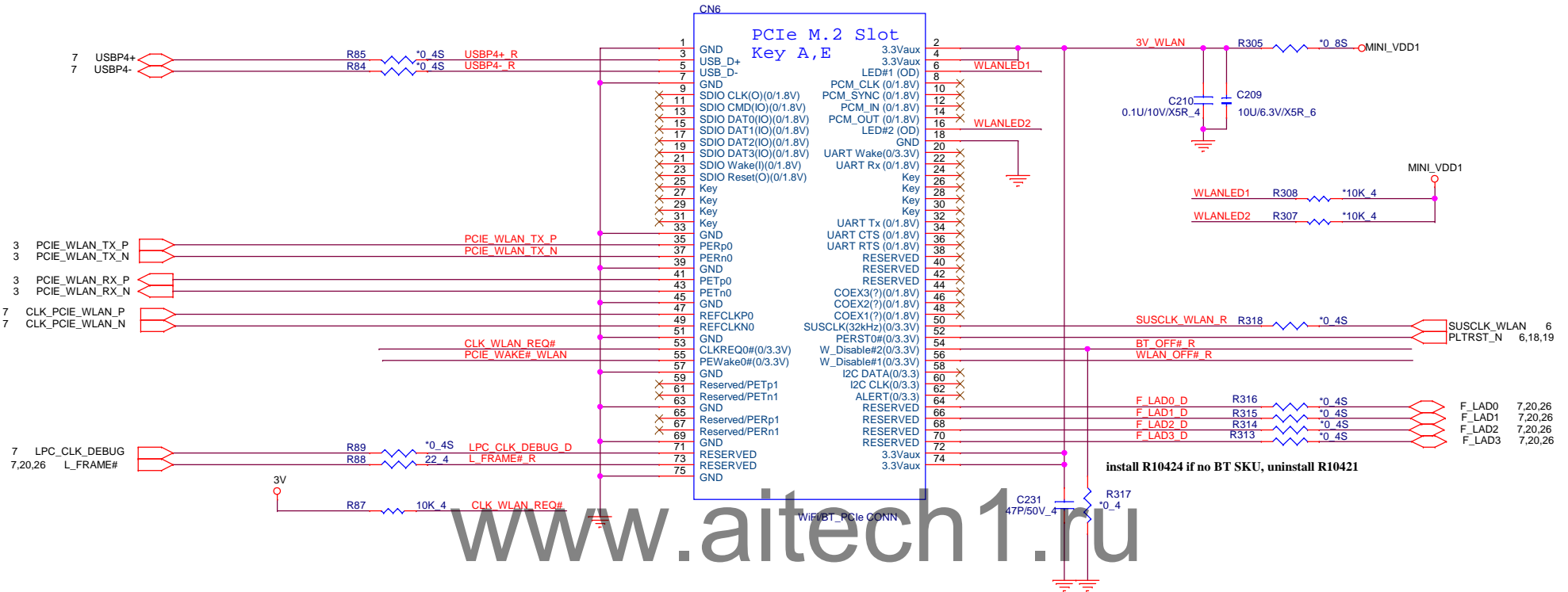
A ground symbol is connected to pin 5.

 PROJECT Compressor Quanta Computer Inc.			
Size	Document Number		Rev
	USB2.0/USB3.0 Conn	799918-000	A1A
Date:	Monday, January 26, 2015	Sheet	22 of 44

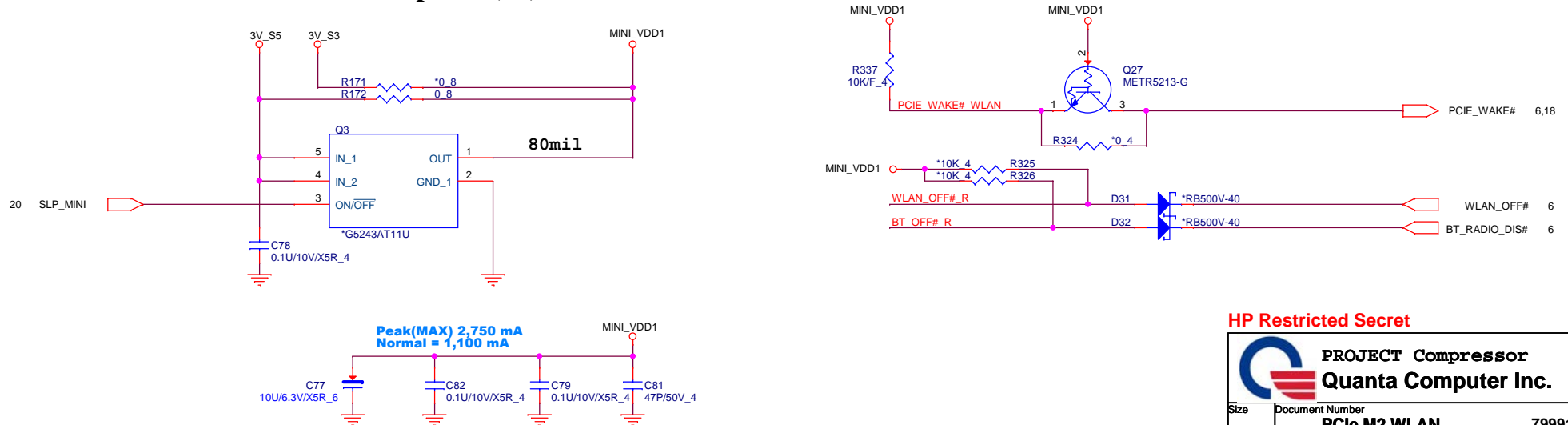
PCIe M.2 Slot Key A,E

H=9.0

23



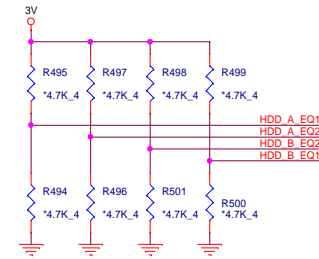
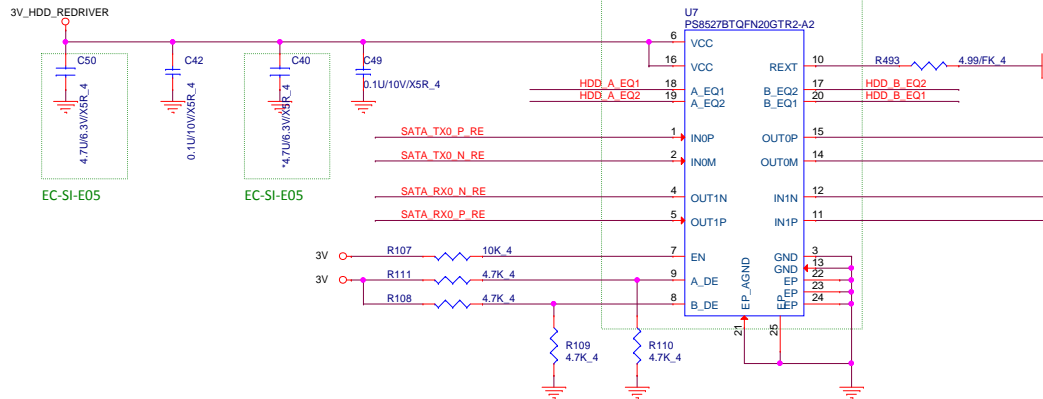
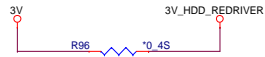
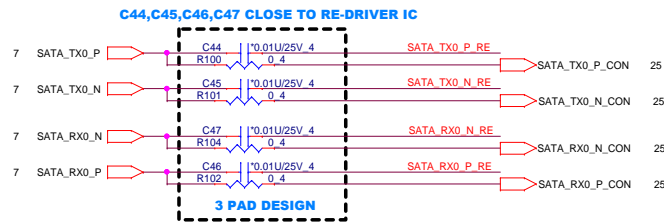
PCIe M2_power(S5)



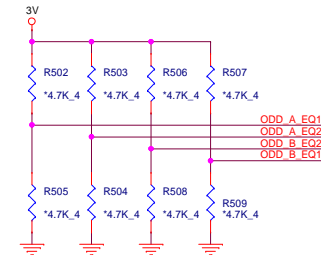
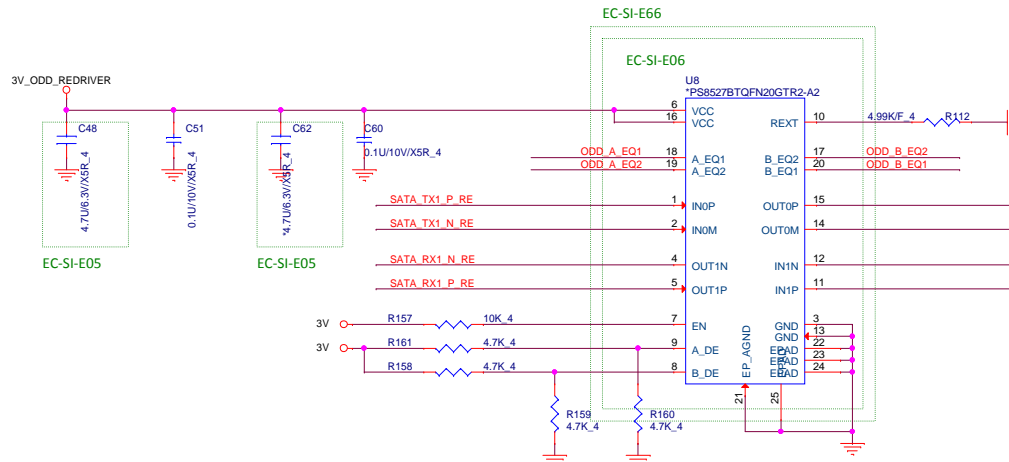
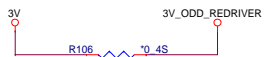
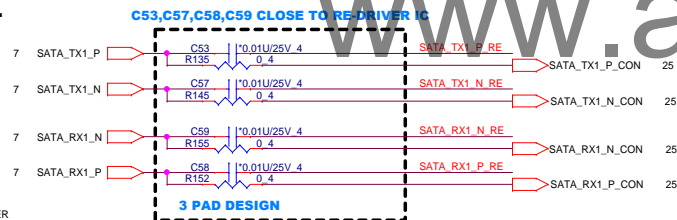
HP Restricted Secret

		PROJECT Compressor	
		Quanta Computer Inc.	
Size	Document Number	799918-000	Rev
	PCIE M2 WLAN		A1A
Date:	Monday, January 26, 2015	Sheet	23 of 44

HDD REDRIVER



ODD REDRIVER



HP Restricted Secret

The diagram illustrates the PCB layout for a SATA HDD connector, featuring two main connector types: **3 PAD DESIGN** and **DIP_H type**.

3 PAD DESIGN: This section shows the connection of the SATA HDD connector (CN7) to the SATA_TX0_P_CON, SATA_TX0_N_CON, SATA_TXN0_R, SATA_RX0_N_CON, SATA_RXN0_R, SATA_RX0_P_CON, and SATA_RXP0_R signals. The signals are routed through a series of pads and vias, with component values such as 0.01U/25V_4 and 0.01U/25V_4 specified for the pads. The signals are connected to the SATA_TX0_P_CON, SATA_TX0_N_CON, SATA_TXN0_R, SATA_RX0_N_CON, SATA_RXN0_R, SATA_RX0_P_CON, and SATA_RXP0_R pins of the connector.

DIP_H type: This section shows the connection of the SATA HDD connector (CN5) to the SATA_HDD_PWR and SATA_HDD_GND signals. The signals are routed through a series of pads and vias, with component values such as 0.01U/25V_4 and 0.01U/25V_4 specified for the pads. The signals are connected to the SATA_HDD_PWR and SATA_HDD_GND pins of the connector.

The diagram also shows the connection of the SATA HDD connector to the SATA_TX0_P_CON, SATA_TX0_N_CON, SATA_TXN0_R, SATA_RX0_N_CON, SATA_RXN0_R, SATA_RX0_P_CON, and SATA_RXP0_R signals. The signals are routed through a series of pads and vias, with component values such as 0.01U/25V_4 and 0.01U/25V_4 specified for the pads. The signals are connected to the SATA_TX0_P_CON, SATA_TX0_N_CON, SATA_TXN0_R, SATA_RX0_N_CON, SATA_RXN0_R, SATA_RX0_P_CON, and SATA_RXP0_R pins of the connector.

The schematic diagram illustrates the internal circuitry of the SATA-to-USB adapter board. Key components include:

- Connectors:**
 - CN9:** SATA connector with pins 1-7 and ground pins 8, 9.
 - CN12:** USB connector with pins 1-4.
- Capacitors:**
 - C67:** 22u/10V/X5R_8
 - C66:** 68P/50V_4
 - C64:** 0.1u/10V/X5R_4
 - C63:** 10u/10V/X5R_8
- Diode:** D2, a TVS DIODE.
- Resistor:** F3, 0.12S.
- Power and Ground:** 5V ODD power supply and various ground connections.
- Dimensions:** 80MIL spacing is indicated for the USB connector pins.
- Component Callouts:**
 - SATA-ODD:** Includes part numbers like sata-c12712-10704-I-7p-r and DFHS07FR023.
 - SATA-ODD-PWR:** Includes part numbers like 50273-0047h-001-4p-I and DFHD04MR296.

0.26 PWRBTN#
20 PWR_ON_LED#

5V S5

EC-SI-E55

F7
QB/POLY_SW 6V/1.1A

2

PWRBTN#

PWR_ON_LED#

CN11

4
3
2
1

POWER_B

AD9
TVS DIODE

AD8
TVS DIODE

EMI reserve

5V S5

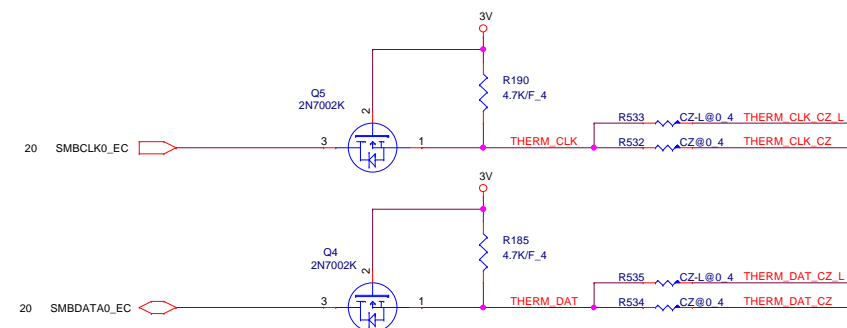
C387
220P/50V_4


C388
220P/50V_4

C386
220P/50V_4

PWRBTN#

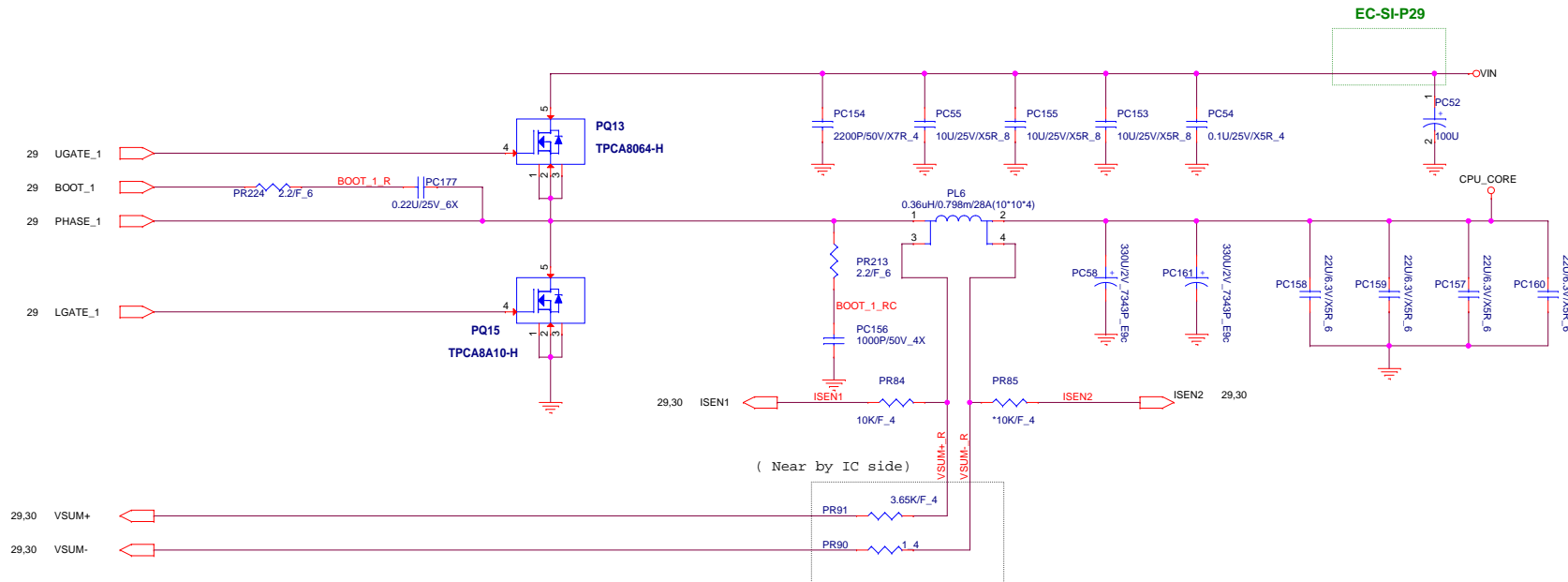
PWR_ON_LED#

[illegible][illegible][illegible]

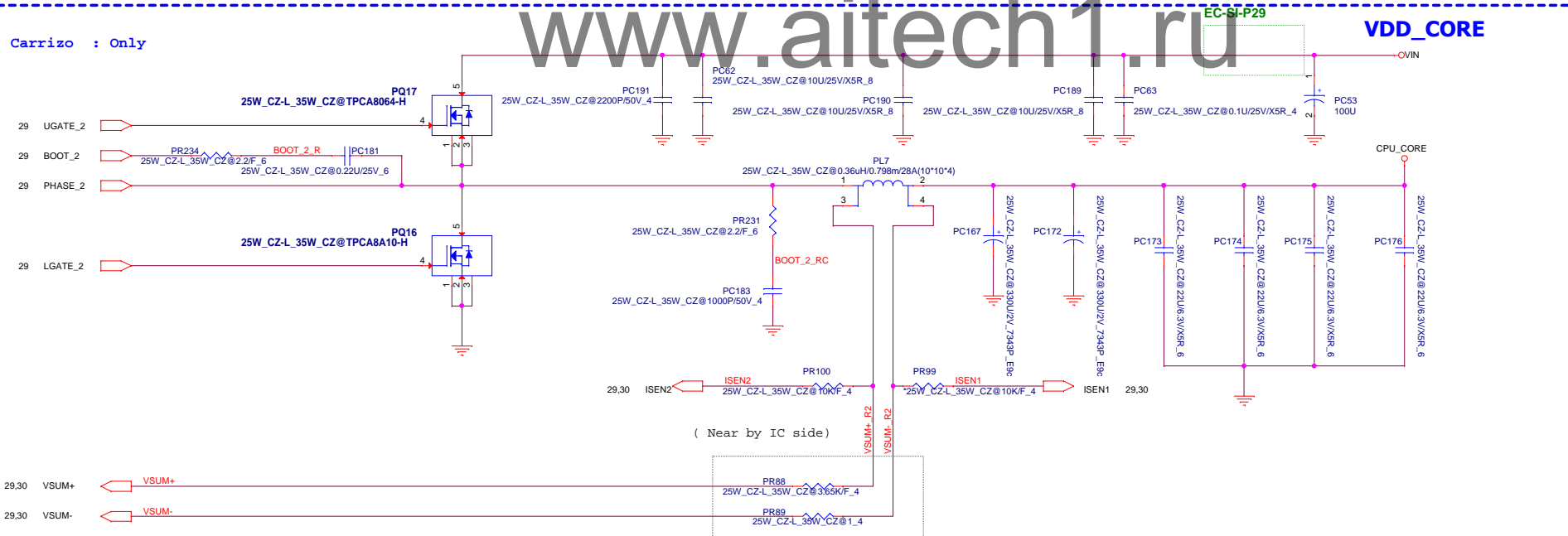
 PROJECT Compressor Quanta Computer Inc.		
Size	Document Number	Rev
	FAN/HDD/ODD/POWER BUT CONN. 799918-000	A1A
Date:	Monday, January 26, 2015	Sheet 25 of 44



Add 9 GND VIAS for thermal pad



Carrizo : Only



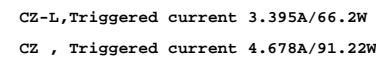
HP Restricted Secret


TDC = 12A
EDC = 17A
OCP= 22A

(Peak 17A)

Frequency: 300KHz





 PROJECT Compressor Quanta Computer Inc.	
Size	Document Number DC-IN 799918-000
Date: Monday, January 26, 2015	Sheet 32 of 44 Rev A

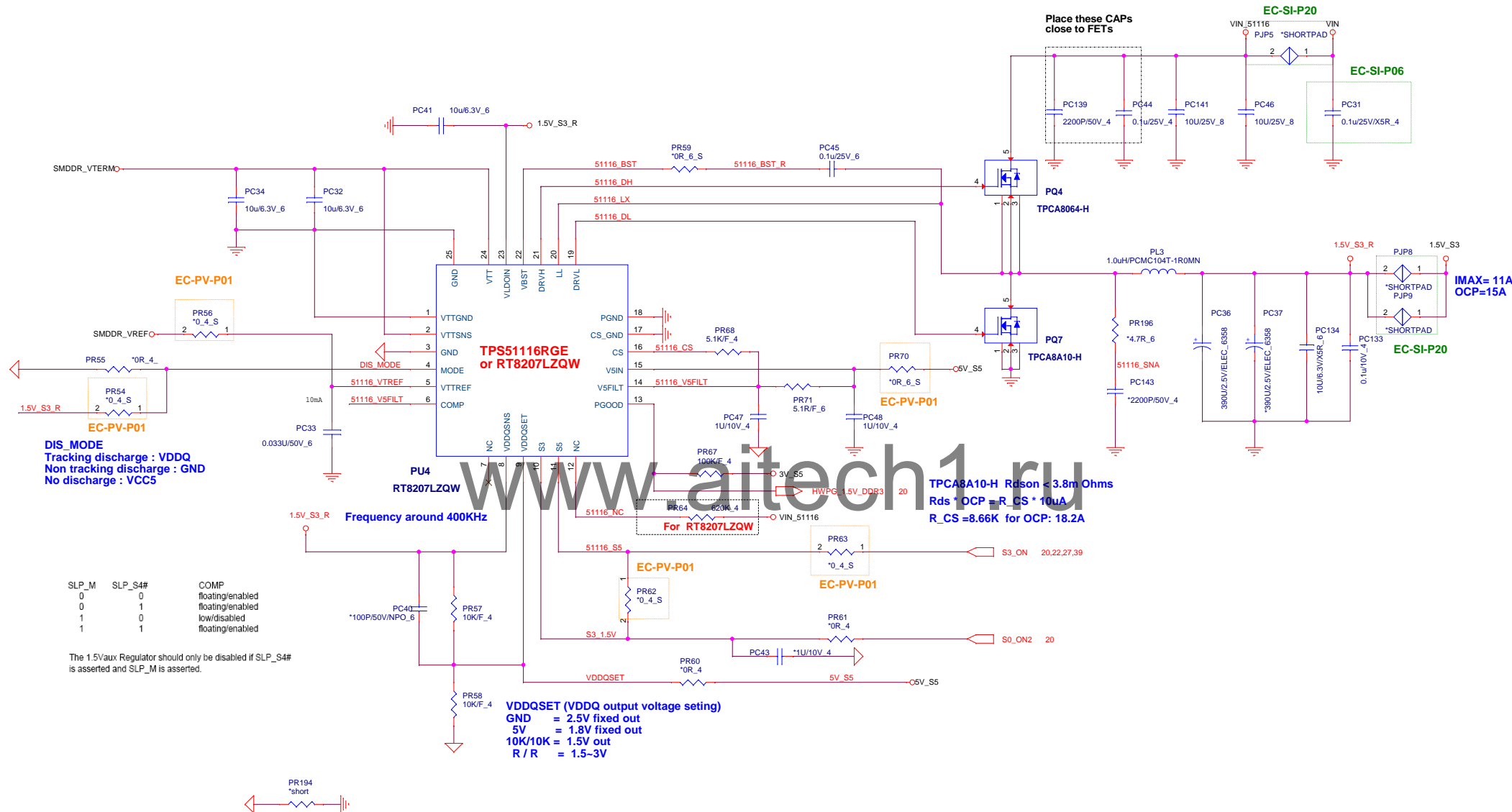




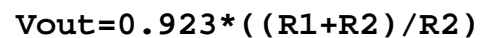
DDR POWER --1.5VSUS&VTT

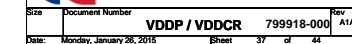
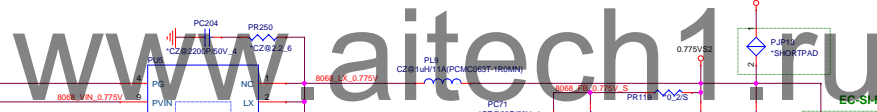
10,11,12,13,39 SMDR_VTERM
10,13 SMDR_VREF
22,25,27,29,32,33,37,38,39 5V_S5
4,8,10,11,12,13,38,39,40 1.5V_S3
16,28,30,31,32,34,36,37,39,40 VIN
6,7,8,10,13,16,18,20,23,26,32,33,36,37,38,39 3V_S5

35

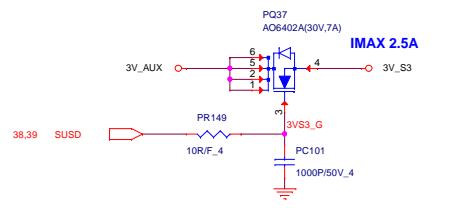
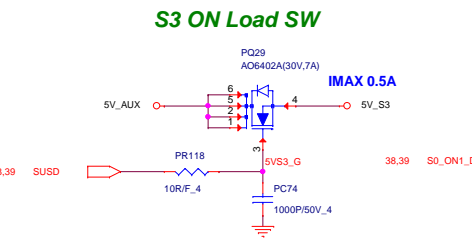


HP Restricted Secret



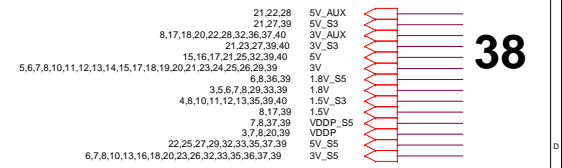
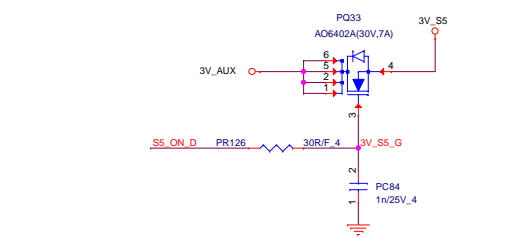
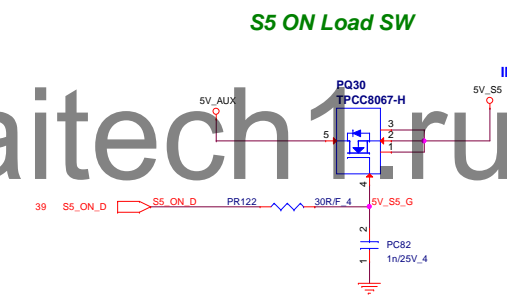
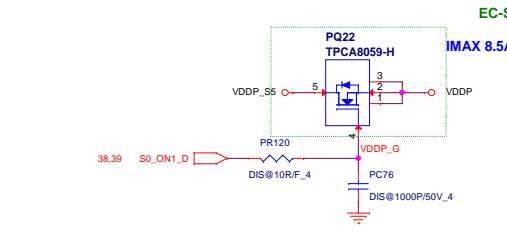
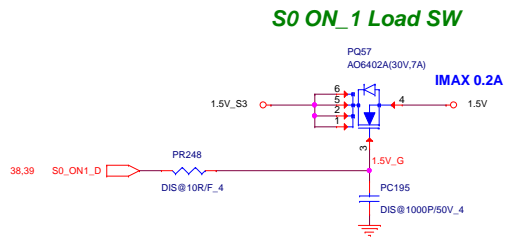
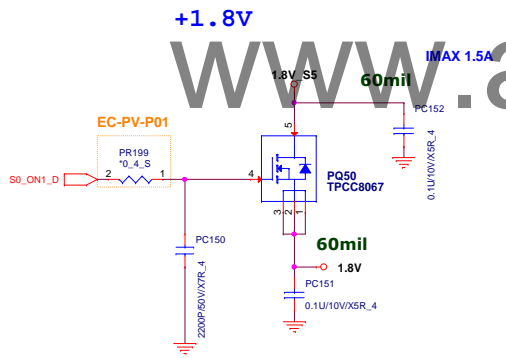
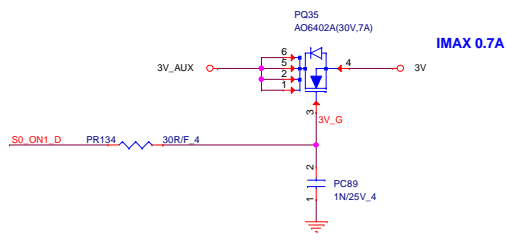
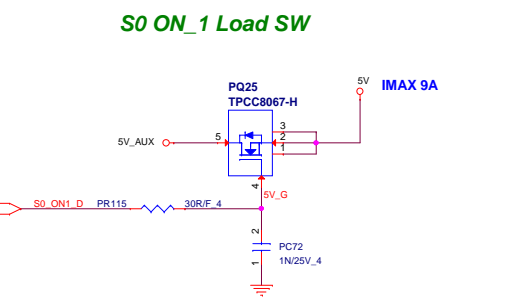


Load Switch



Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
AO6402A	TSOP-6	5.0A/6.7A	42m	+/- 20V
TPCC8067-H	3x3	9A	26m	+/- 20V
TPCA8A10-H	SO-8	20A	7.9m	+/- 20V

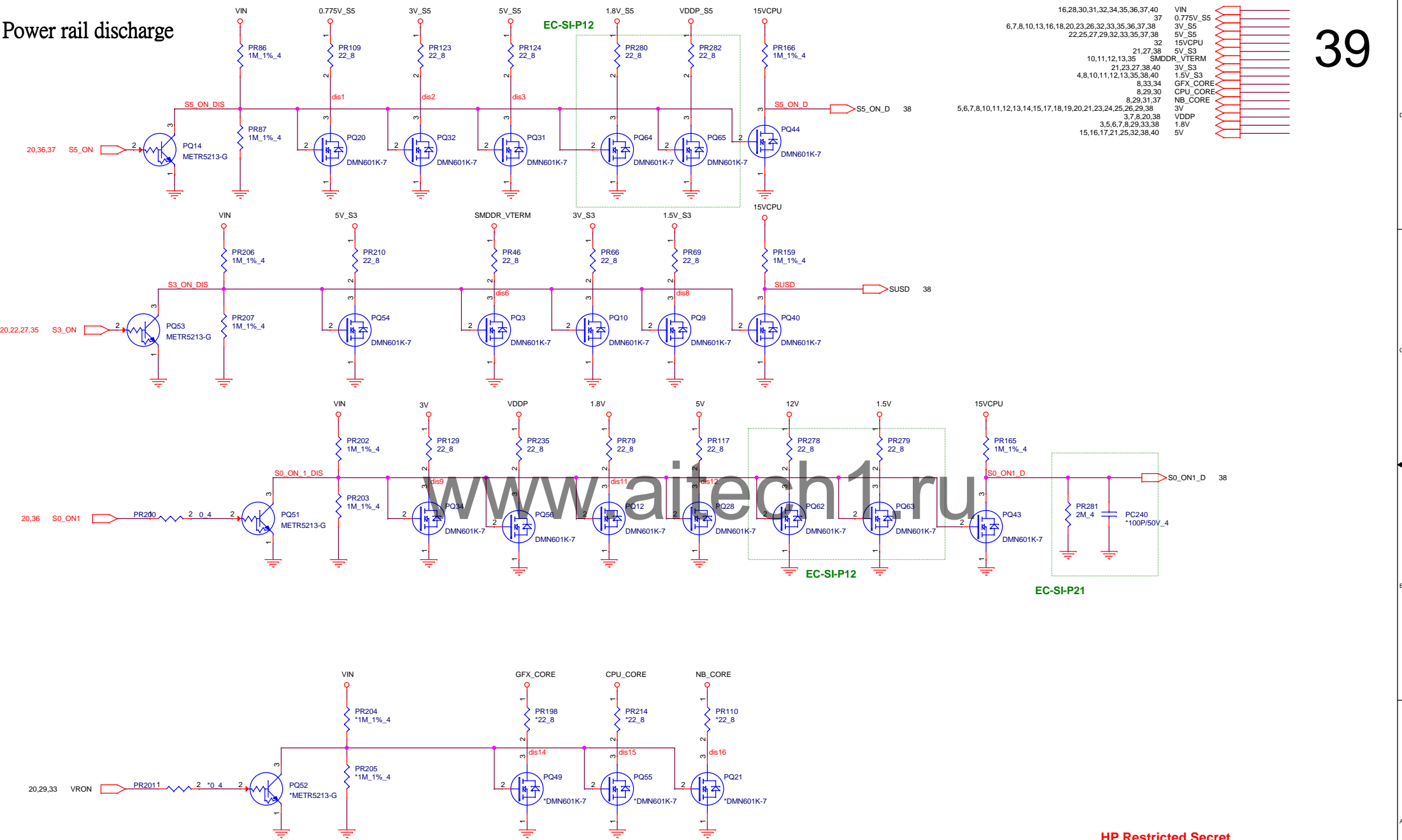


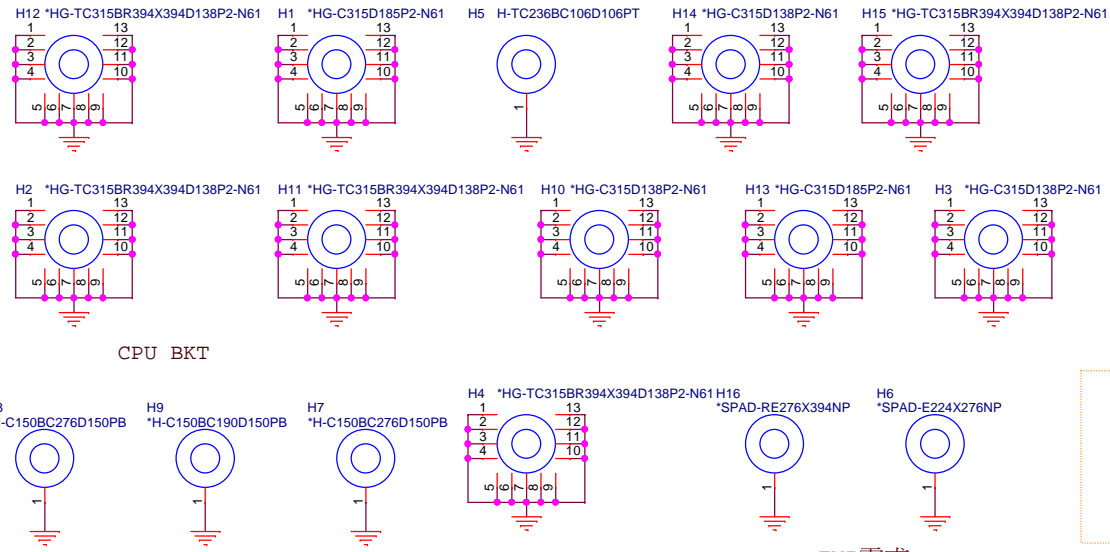
HP Restricted Secret

PROJECT Compressor
Quanta Computer Inc.

Size	Document Number	Rev
	Load Switch	799918-000
Date	Monday, January 26, 2015	Sheet 38 of 44

Power rail discharge



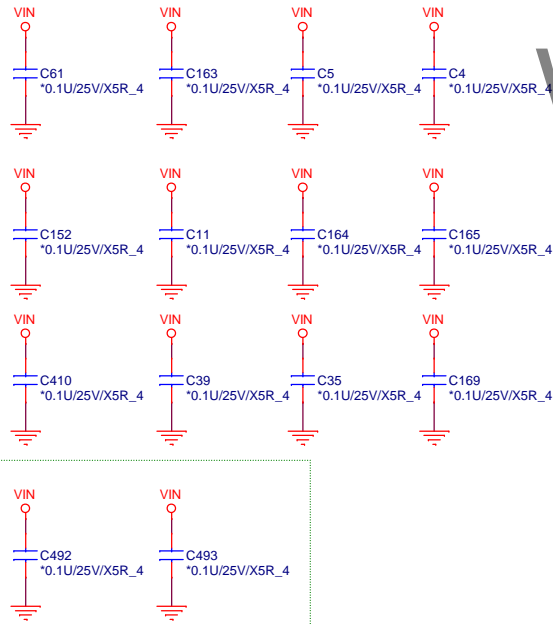


CPU BKT

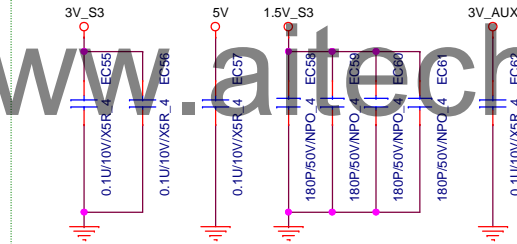
EC-SI-E62

EMI 需求

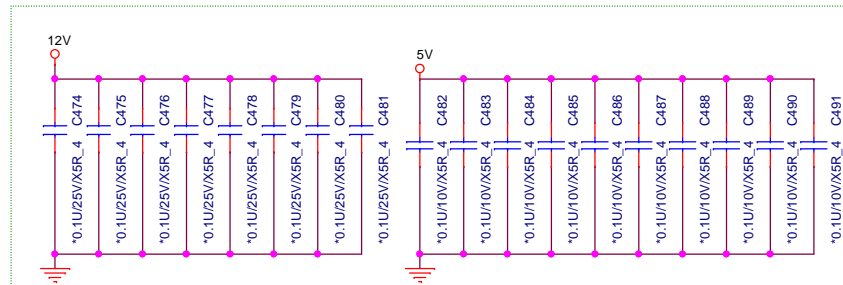
EC-PV-E11



EC-SI-E64




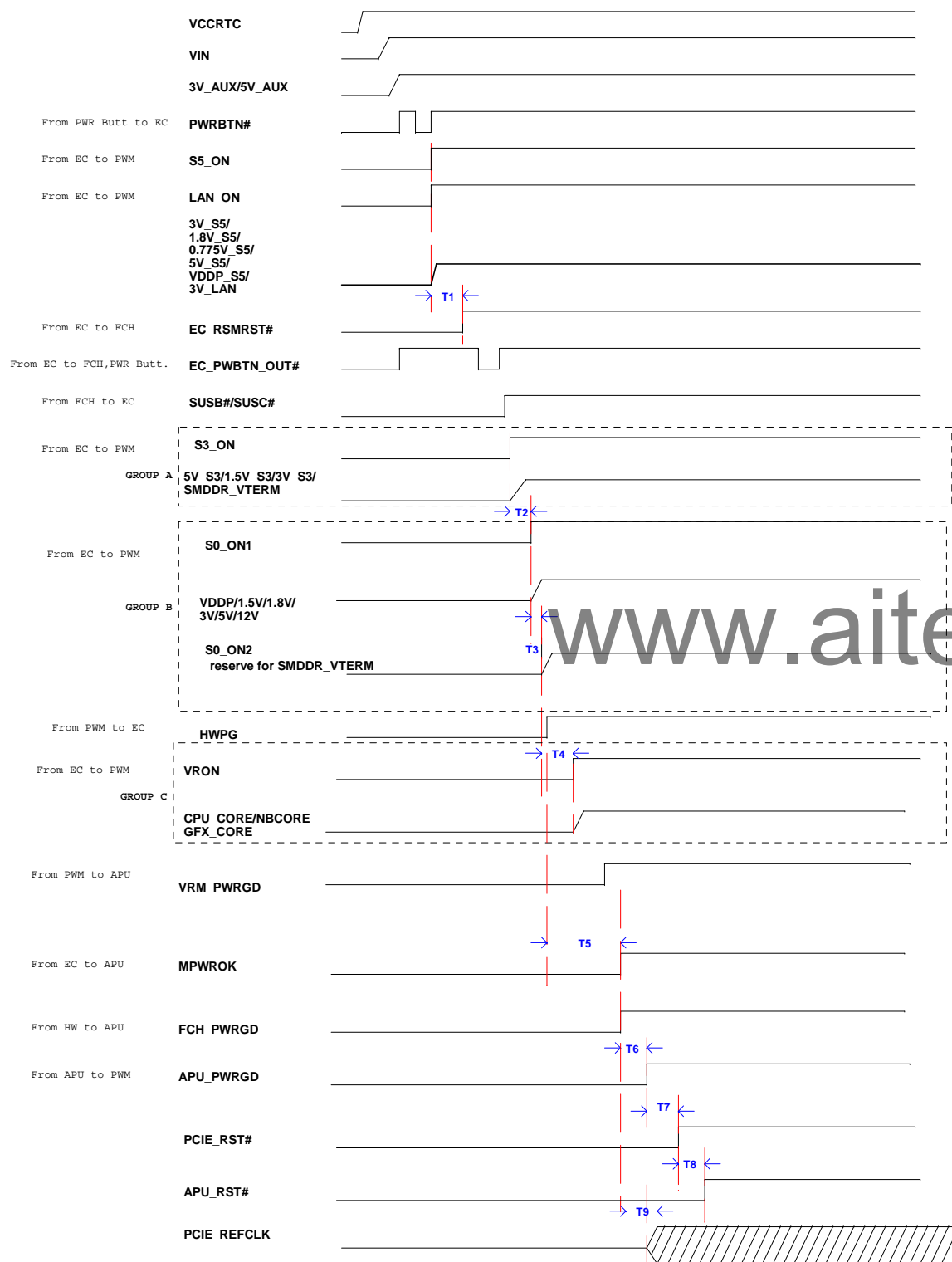
EC-SI-E47



EC-SI-E61

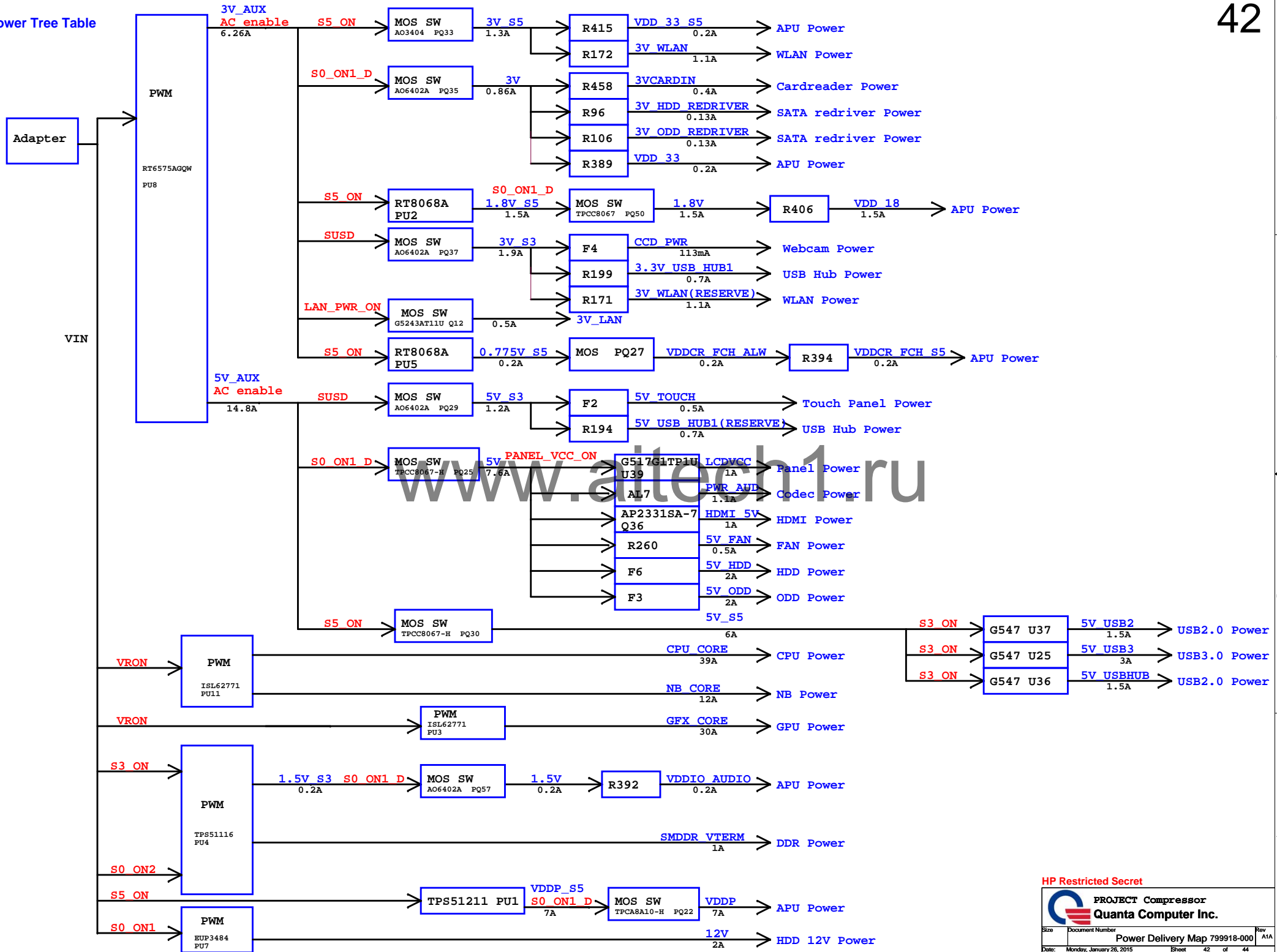
HP Restricted Secret

				
<div>PROJECT Compressor</div> <div>Quanta Computer Inc.</div>				
Size	Document Number			Rev
	HOLE			A1A
	799918-000			
Date:	Monday, January 26, 2015	Sheet	40 of 44	

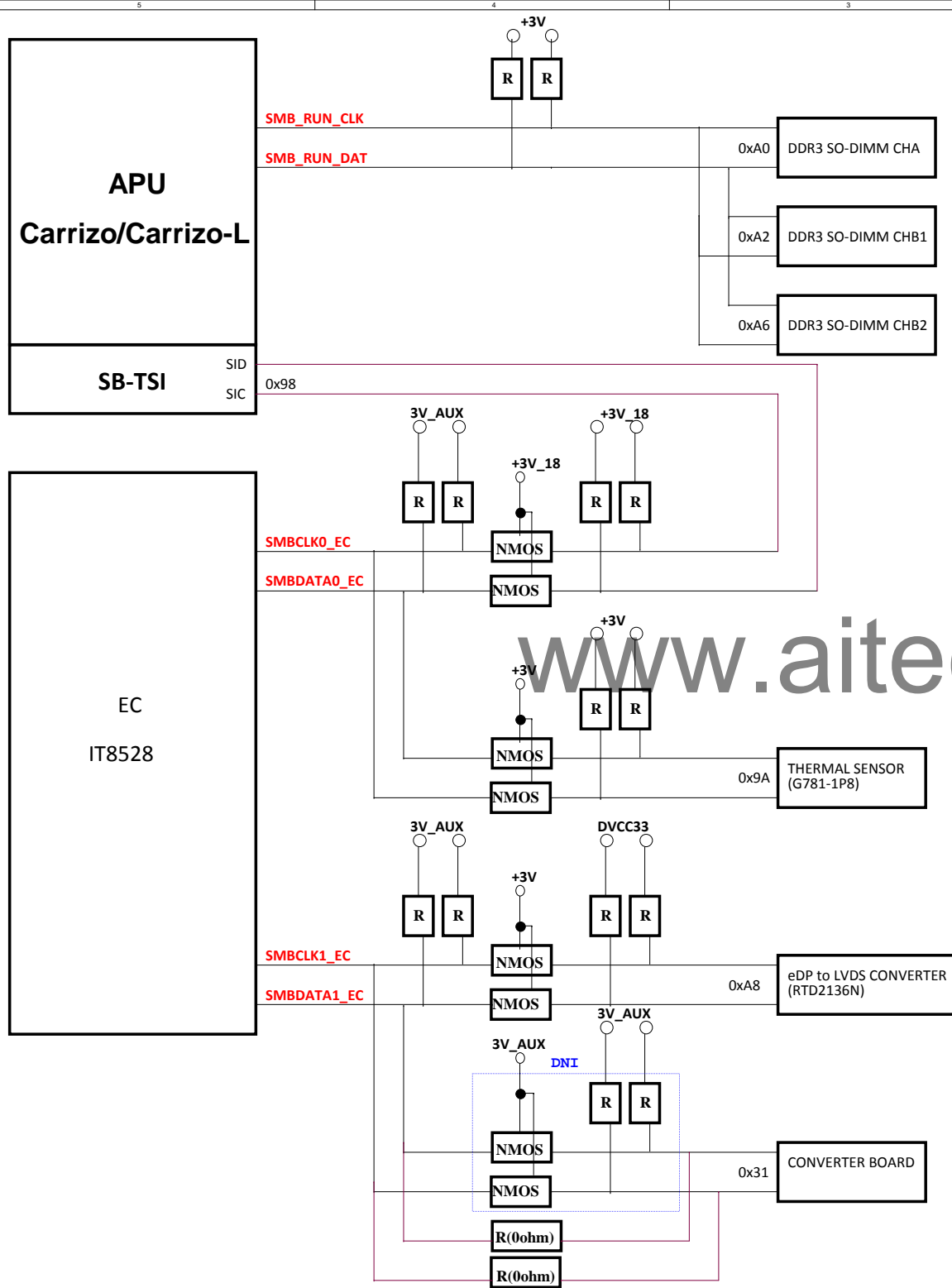


System Power Sequence	
EC Control:	
T1: S5_ON TO EC_RSMRST#	= 20ms
T2: S3_ON TO S0_ON1	= 10ms
T3: S0_ON1 TO S0_ON2	= 1ms
T4: S0_ON2 TO VRON	= 10ms
T5: HWPG TO MPWROK	= 50ms
Timing spec:	
T1 Spec:	10ms min
Power Up Spec:	
Group A > Group B > Group C	
T6: FCH_PWRGD TO APU_PWRGD	= 108.6 ~ 118.6 ms
T7: APU_PWRGD TO PCIE_RST#	= 114.2 ~ 124.2 ms
T8: PCIE_RST# TO APU_RST#	= 111.9 ~ 121.9 ms
T9: FCH_PWRGD TO PCIE_REFCLK	= 37.6 ~ 47.6 ms

Power Tree Table



HP Restricted Secret



HP Restricted Secret

DB to SI Change List

EC-SI-E01 Change BOOT_BLK_WR_EN# from AGPIO102 to AGPIO72 -- Page 6

EC-SI-E02 Add 1K to WC_DETECT# and PANEL_ID0, ID1, ID2

EC-SI-E03 C17 change to 0805 size, C417 change to 1808 size, EC13/EC14 change to 0402 size

EC-SI-E04 Add co-lay resistor R473-R492 to LVDS interface

EC-SI-E05 C1, C32, C117, C131, C411, C416 change to 0402 size

EC-SI-E06 Change SATA re-driver solution

EC-SI-E07 Add one gpico for EC to distinguish CZ and CZ-L

EC-SI-E08 Change HUB IC P/N to AL00850G004

EC-SI-E09 Change GEVENT2# from Pull high 10K to PD 2K

EC-SI-E10 AGPIO8/40 need pull up to 3V_S5 if no use on CZ

EC-SI-E11 GENINT1_L/AGPIO89(HVBEN_L):Connect to VSS to enable, or if not used, leave unconnected to disable AMD Hardware Validated Boot.

EC-SI-E12 R143/R121/R142/R151 change to 10K to meet SCL

EC-SI-E13 Pop R431 for SPI WP#

EC-SI-E14 Change PWR_GOOD pull up power domain to 3V & 1.8V (S0 state) for SCL ver. 1.04

EC-SI-E15 SPI_CS2_L/ESPI_CS_L/EGPIO119 need pull up to 1.8V if no use on CZ

EC-SI-E16 Exchange CN15 pin define between pin 1 and pin 30 for cable routing change

EC-SI-E17 Reserve 0ohm to 3V_S5 instead LAN power switch if needed

EC-SI-E18 un-pop C144, pop C432, C139 to follow CRB

EC-SI-E19 un-pop Q30 that only workaround for SharkBay platform's RTC logic latch issue.

EC-SI-E20 Change VDDP_GFX power rail from VSS to VDDP that depop R332, add R523, C438 and C439 fixed PCI-E Device no function and system reboot failure issues.

EC-SI-E21 Add D38 unpop Q24 reserve RSMRST#_R level

EC-SI-E22 Pop D30 for HW power good control.

EC-SI-E23 Unpop R54 and pop R46 for HDMI no output.

EC-SI-E24 Add 0ohm R524 to GND for Interlace mode selection

EC-SI-E25 Change C37 and C38 from 6.8uF to 5.6uF as vendor recommend.

EC-SI-E26 Reserve 0ohm R525 for VRM_GFX_PWRGD inform system.

EC-SI-E27 Change Q715 net from HDMI_MB_HP_L1 to HDMI_MB_HP_L due to same netname.

EC-SI-E28 CLKREQ0 only Carrizo need pull up if no use and CLKREQ1,2 change to depop if no use.

EC-SI-E29 USB_OC5/6/7 only for Carrizo only , so cna't use for Carrizo/Carrizo-L co-lay design, R327,R341,R354,R356 depop. U3B_OC change to OC1,Charger_OC change to OC2 and HUB_OC combine to U2B_OC

EC-SI-E30 SD0_LED/EGPIO93 need PU for Carrizo-L only if no use.

EC-SI-E31 LPC_PD_L/AGPIO21 need PU if no use.

EC-SI-E32 R330 need PU for Carrizo and Carrizo-L

EC-SI-E33 C440 add for across the VDDIO_MEM_S3 and VSS plane split.

EC-SI-E34 VDDP add five 0.22u for SCL ver. 1.05 update.

EC-SI-E35 C304 change to 0.22u for SCL ver. 1.05 update.

EC-SI-E36 Add 0.1u C446, C447 for 0.75V_VREF_CA and 0.75V_VREF_CA_A0 power quality.

EC-SI-E37 Change C15 to 1210 size and pop C66 68pF, C67 22uF for RF solution.

EC-SI-E38 Non-Install AR22, AR26, AQ5, AQ6, AQ4, AQ3, AR17, AR18, AR20 and AC30 for audio noise issue from resume S3.

EC-SI-E40 Add 10uF*4 and reserve 8pF*4 on CPU_CORE to GND for RF solution.

EC-SI-E41 Add 10uF*6 and reserve 8pF*6 on DDR D1W4 1.5V_S3 to GND for RF solution.

EC-SI-E42 Pop 120ohm on R188, R189, R202, R203 for EMI solution

EC-SI-E43 Add R530, R528, U40, R531, R529, C469, C470, Q40, R532-R535 for thermal move ambient sensor of CZ-L

EC-SI-E44 Add R537 and R538 for APU TDP ID pin.

EC-SI-E45 Add R539 pull high for SATA LED leakage.

EC-SI-E46 Change U39 from sot-23-5 to tsot-23-6 for larger current limit.

EC-SI-E47 Add two 0.1u from 3V_S3 to GND. Add one 0.1u from 5V to GND. Add four 180p from 1.5V_S3_S3 to GND. Add one 0.1u from 3V_AUX to GND for EMI solution

EC-SI-E48 Change LVDS signal 0ohm to common mode choke for EMI solution

EC-SI-E49 depop R83 to meet SCL V1.05

EC-SI-E50 pop AD3/AD4/AD6/AD7/U1/U4/U19/U23 for ESD solution

EC-SI-E51 Change BT1 footprint and part number for SMT requirement and HP service requirement

EC-SI-E52 Change C22/C23/C234/C322/C431/C91 cap voltage value for Quanta PUR request command part

EC-SI-E53 Reserve C471/C472/C473 for power quality

EC-SI-E54 Change fuse F1/F3/F5/F6 to 0ohm for safety recommend.

EC-SI-E55 Add F7 for ESD protect

EC-SI-E56 Change JDIM1-JDIM4 footprint for SMT requirement

EC-SI-E57 Pop L9/L10/L28-L31 depop R449-R456/R248/R249/R255/R256 for EMI solution

EC-SI-E58 Change CX12B900000 footprint for this part dedicated footprint

EC-SI-E59 pop R384/R419 depop R390/R418 to meet SPI TPM spec

EC-SI-E61 Add eight 0.1u from I2V to GND. Add ten 0.1u from 5V to GND for RF solution

EC-SI-E62 Change the mounting hole design and follow HP recommends.

EC-SI-E63 Change CN15, BT1 material for MR require

EC-SI-E64 Add C492, C493 for across the VIN and VSS plane split.

EC-SI-E65 Reserve damping resistor R541, R542 for FCH_SPI_WP and SPI_HOLD#.

EC-SI-E66 Depop ODD Redrivr U8 due to SATA signal can pass before BIOS fine tune.

EC-SI-E67 Depop R119, R141, R371 for SPI TPM not support.

EC-SI-E68 Change Change CZ-L 3VS5_3VSTRAP from 3V_S5 to 3V to meet SCL V1.05

EC-SI-E69 Change CN24 CN25 change to DFHS09PR11 for main source change , footprint no change

EC-SI-E70 Change R258, PR154 to 330ohm for LED brightness fine tune.

EC-SI-E71 Pop R366, R361 for AMD CRB change due to codec issue that the Audio Codec will not be recognized by the OS.

EC-SI-E72 Depop R176, R177 for USB yellow mark due to new version hub IC remove port disable function.

EC-SI-P01 Change PR184 from short pad to 0402 for HW protection canceling and stuff PR181 and PR182 _0 ohm for Informing EC to support adapter SMART ID function.

EC-SI-P02 PC218 / PC216/PC207 / PC210 change p/n and footprint from CC0805 to CC0603 p/n: CH6101M9905

EC-SI-P03 PC106/ PC99 change p/n and footprint from CC0805 to CC0603 p/n: CH5471M9B00

EC-SI-P04 PR151 change p/n : CS41002FB28

EC-SI-P05 Add 0ohm PR274 For debug

EC-SI-P06 PC31 / PC233 / PC230 / PC237 / PC235 / PC236 / PC117/ PC113/ PC116 change p/n and footprint from CC0603 to CC0402 p/n: CH4104K9B03

EC-SI-P07 PC222 change p/n and footprint from CC0603 to CC0402 p/n: CH5101K9B01

EC-SI-P08 PC223 change p/n and footprint from CC0603 to CC0402 p/n: CH5222K9B06

EC-SI-P09 Depop PC202 / PC203/ PR251 No need on the component

EC-SI-P10 Add PR275/PR276 / PR277 Add pull high resistance for switch gate

EC-SI-P11 Pop PR253 Add pull low resistance for FCH_S5_POWER_COMP

EC-SI-P12 Add PR278/PQ62/PR279/PQ63/PR280/PQ64 Add 12V/1.5V/1.8V_S5 discharge

EC-SI-P13: change PR127 / PR128 / PR256 / PR257 /PR125/PR116 footprint

EC-SI-P14: change PU6: change p/n , change to push pull op.

EC-SI-P15: change PR132 / PR140 p/n to 1.1K , follow MRB

EC-SI-P16: Remove PR266, Remove reserve resistance.

EC-SI-P17: Add adapter throttling

EC-SI-P18: add PD10 for inrush voltage

EC-SI-P19: add OP second source

EC-SI-P20: change RJP1-RJP20 footprint from open to short.

EC-SI-P21: add PR281 / PC240 reduce Vgs in VDDP/ 1.5V load SW.

EC-SI-P22: Modify PR146 to 62K , PR148 to 51K , PR25 to 17K for 5V/3V/VDDP_S5 OCP.

EC-SI-P23: Modify PR102 to 1.58K / PC10 modify to 0.22uF for CPU /GFX load line .

EC-SI-P24 change PQ22 p/n to BAM80590000 for leakage

EC-SI-P25 Remove PQ48 / PC128 /PC88 this for battery power saving .

EC-SI-P26 Add PC241 for 0.775V_S5 ripple.

EC-SI-P27 Disable EC6/EC7/EC16/EC17 change EC3/EC4 P/N to CH6224M9A00

EC-SI-P28 Add PR303/PR304 for faster throttling function

EC-SI-P29 Remove RJP10 / RJP11 / RJP4 for placement

EC-SI-P30 Change PL8 / PL4 / PL5 part number Buyer suggest material

EC-SI-P31 No stuff PU10 for remove AC lost protection circuit.

EC-SI-P32 Add PC 242 by pass capacitor for amp. power.

HP Restricted Secret

PROJECT Compressor			
Quanta Computer Inc.			
Size	Document Number	799918-000	Rev A1A
Change list			
Date:	Monday, January 26, 2015	Sheet 44 of 44	